Spartan-6 FPGA Development Board AX309 User Manual

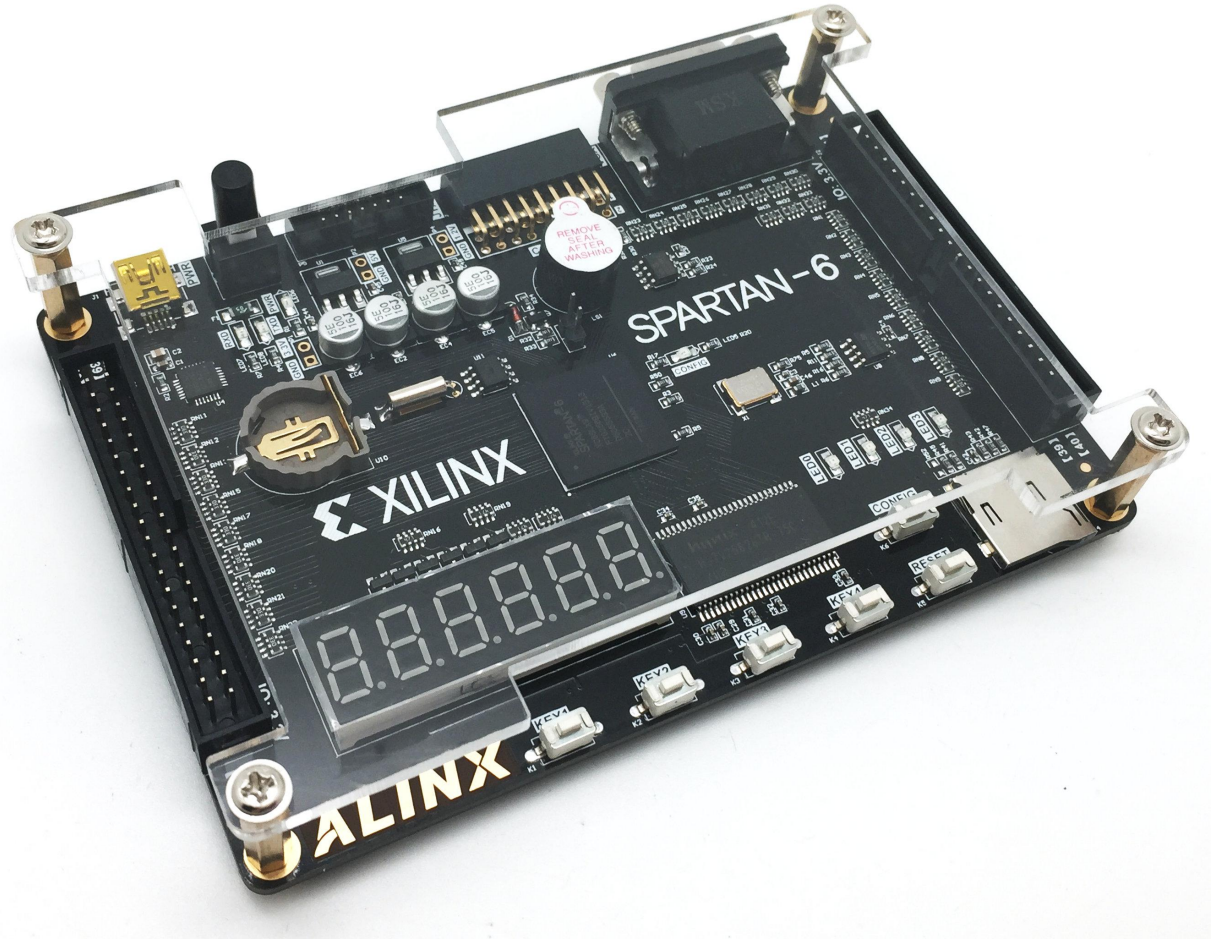
ALINX

Version Record

Version	Date	Release By	Description
Rev 1.0	2019-04-26	Rachel Zhou	First Release

Table of Contents

The FPGA development board (AX309) is an entry-level product, mainly for FPGA beginners. The FPGA development board uses the XILINX SPARTAN6 family chips, model XC6SLX9-2FTG256C, in a 256-pin FBGA package. The entire development board is practical and has two ALINX standard expansion ports. There are 34*2=68 IOs in total. It also brings out 5V power supply, 3.3V power supply, and multiple GND. For engineers who like DIY. , is a very good choice. In addition, many of ALINX's modules can be directly connected to the expansion port of the FPGA development board AX309, such as ADDA module, 4.3-inch LCD screen, audio module, camera module, etc., providing more choices for engineers to learn. Below we will give a detailed introduction to the AX309.



Part 1: FPGA Development Board Introduction

This board is the evaluation board with Xilinx FPGA Spartan-6 used for a complete and powerful system processing. The FPGA chipset is Xilinx Spartan-6 XC6SLX9 device in FBGA256 package, the feature summary of this FPGA device are listed below:

Device	Logic Cells(1)	Configurable Logic Blocks (CLBs)			DSP48A1 Slices(3)	Block RAM Blocks		CMTs(5)	Memory Controller Blocks (Max)(6)	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices(2)	Flip-Flops	Max Distributed RAM (Kb)		18 Kb(4)	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358

Table 1-1: The Feature Summary of FPGA Device

The main resources and features are listed (see Table 1-2):

Parameter	Value
Logic Cells	9152
DSP48 Slices (18 x 18 multiplier, an adder, and accumulator)	16
Configurable Logic Blocks(CLBs)	90Kb
Block RAM Blocks	576Kb
CMTs	2
MAX User I/O	200
Core Power Supply	1.15V-1.25V(suggest is 1.2V);
Operation Temperature	0-85℃

Table 1-2: The Main Resources and Feature of Xilinx Spartan6 XC6SLX9

The layout of the board that indicates the location of the connector and key components, provide a quickly overview of AX309 board (see Figure 1-2)

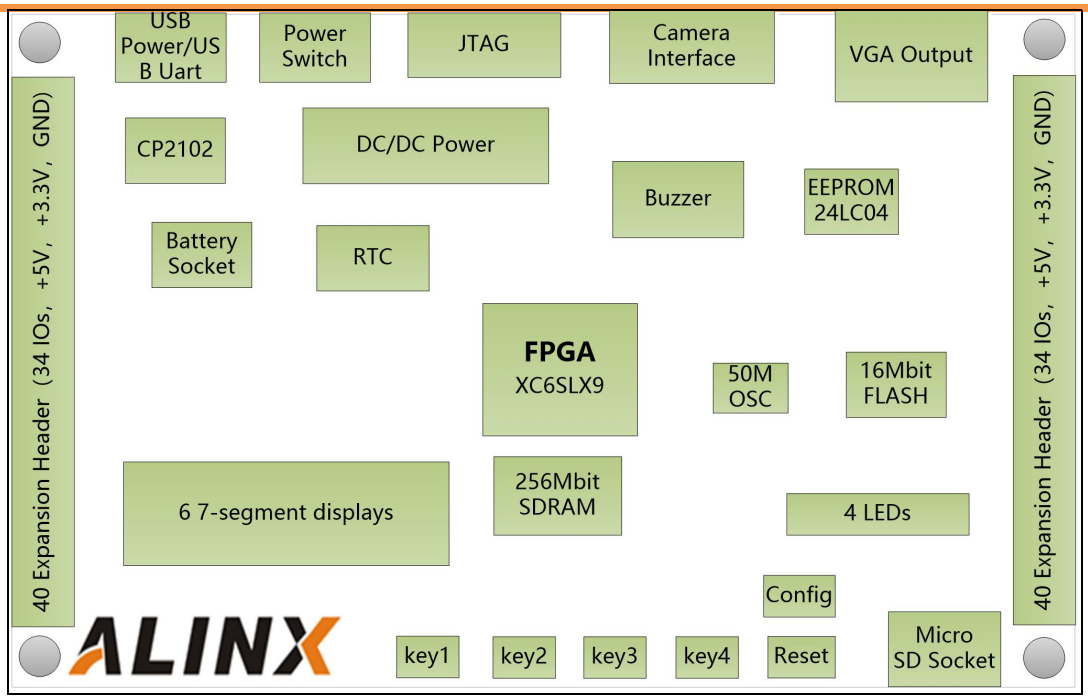


Figure 1-2: The Layout of the AX309 board

Through this diagram, we can see the functions that the development platform can achieve.

- USB interface power supply, and realize USB to serial port function at the same time
- A large-capacity 256Mbit SDRAM can be used as a buffer for data;
- A 16Mbit SPI FLASH that can be used as a storage for FPGA configuration files and user data
- A camera module interface that can connect 5 million OV5640 camera
- One-port VGA interface, VGA interface is 16bit, can display 65,536 colors, can display color pictures, etc
- A piece of RTC real time clock with battery holder, battery model CR1220
- One piece of IIC interface EEPROM 24LC04
- 4 red LEDs for water light function
- 4 independent user buttons
- On-board 50M active crystal oscillator provides stable clock source for

FPGA development board

- 2-Way 40-pin ALINX expansion port (0.1”inch), 34 IO ports, one 5V power supply, two 3.3V power supplies, three GND. Two expansion modules can be connected at the same time, such as expansion modules such as 4.3-inch TFT module and AD/DA module.
- Reserved JTAG port for FPGA debugging and program curing
- One way Micro SD card holder, support SPI mode
- One 6-digit digital tube, 6-digit dynamic display

Part 2: Power

AX309 board is powered by MINI USB port from PC. When the FPGA development board and PC computer are connected with mini USB cable, the AX309 board will power on if the power switch is pushed down. The block diagram of power design as below (see Figure 2-1)

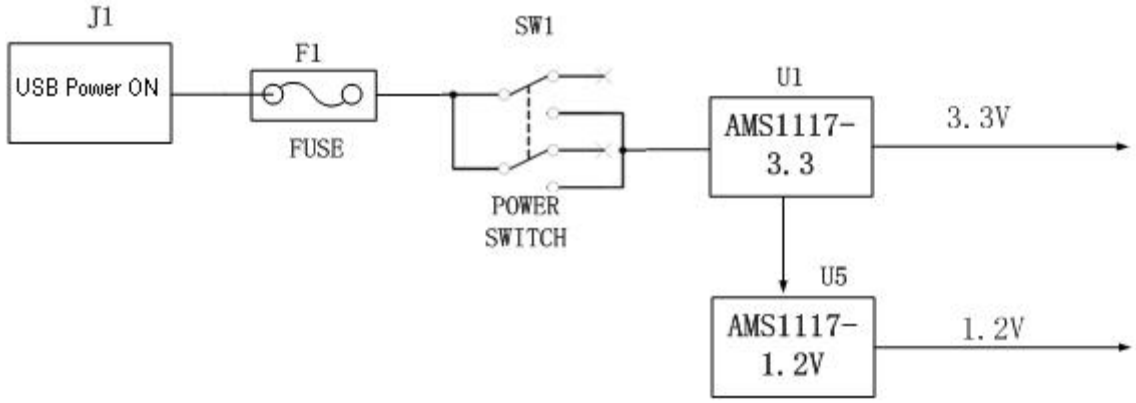


Figure 2-1: Block Diagram of Power Design

The FPGA development board is powered by USB, and generates two +3.3V, +1.2V power supplies through two LDO power chips to meet the BANK voltage and core voltage of the FPGA.

When designing the PCB, we used a 4-layer PCB and reserved a separate

GND layer, so that the entire development board has a complete ground plane, which ensures the development board has very good stability. On the PCB we have reserved test points for each power supply so that the user can confirm the voltage on the board.

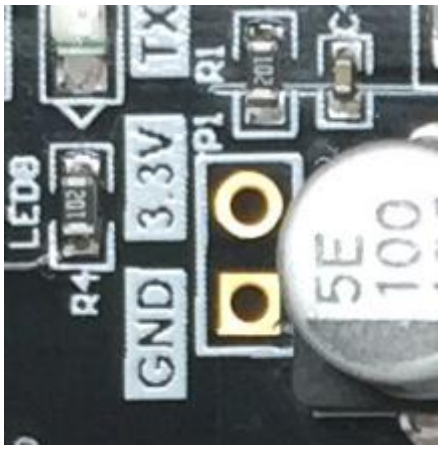


Figure 2-2: The Test Point of Power Voltage

Part 3: FPGA Chip

As mentioned earlier, the FPGA model we use is XC6SLX9-2FTG256C, which belongs to Xilinx Spartan-6. This model is a BGA package with 256 pins. Again, explain the definition of the FPGA pin. Many people use FPGAs that are not BGA-packaged, such as 144-pin, 208-pin FPGA chips. Their pin definitions are made up of numbers, such as 1 to 144, 1 to 208, etc., and when we use BGA packages. After the chip, the pin name becomes in the form of letters + numbers, such as E3, G3, etc., so when we look at the schematic, we see the letters + numbers, which represent the pins of the FPGA. Having said this, let's look at the functions of the various parts of the FPGA.

Figure 3-1: FPGA Chipset

Part 3.1: JTAG Interface

First, let's talk about the FPGA configuration and debug interface: the JTAG interface. The function of the JTAG interface is to download the compiled program (.bit) to the FPGA or download the FLASH configuration program (.mcs) to the SPI FLASH. After the Bit file is downloaded to the FPGA, it will be lost after power-off. It needs to be powered on and downloaded again. However, after downloading the MCS file to FLASH, it will not be lost after power-off. After power-on, the FPGA will read the configuration file in FLASH and run it.

The hardware design of JTAG connector is showed as Figure 3-2, JTAG interface includes four signals (TCK,TDO,TMS,TDI). these four signals connects between FPGA device and JTAG connector with 33ohm resistors, the 33ohm resistors will protect FPGA device to avoid damage。

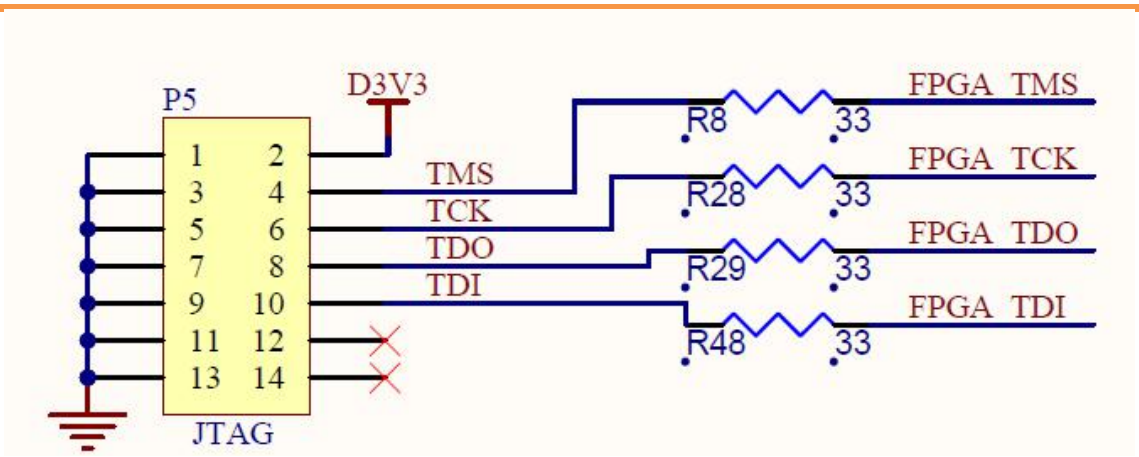


Figure 3-2: Hardware Design of JTAG Connector

JTAG connector is 14pin connectors, the pin pitch is 2.0mm.

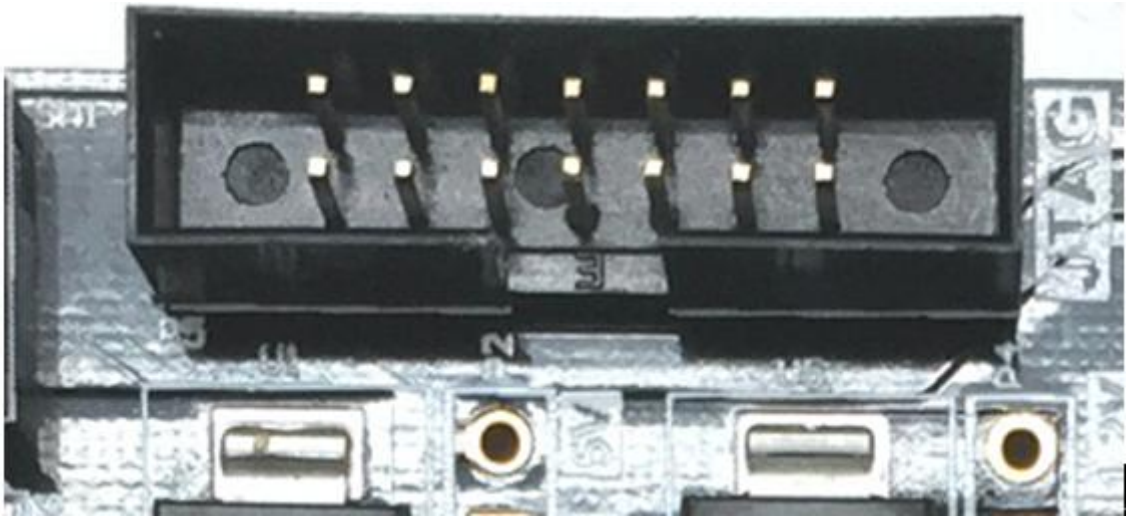


Figure 3-3: Onboard JTAG Connector

Part 3.2: FPGA Power Supply

There are three power supplies for Spartan-6 FPGA including bank voltage (VCCIO), core voltage(VCCINT) and auxiliary voltage(VCCAUX). The VCCINT power supply voltage is +1.2V, VCCAUX voltage can be +3.3V or +2.5V, in AX309 board it is connected to +3.3V. VCCIO is the power supply for each FPGA BANK, where VCCIO0 is the power supply of FPGA BANK0, VCCIO1~VCCIO3 respectively power supply of FPGA BANK~BANK3. In the AX309

board, all of VCCIO pin is connected to +3.3V voltage, so that the IO voltage standard of all bank is +3.3V. Hardware design of FPGA power pin is showed as following Figure 3-4:

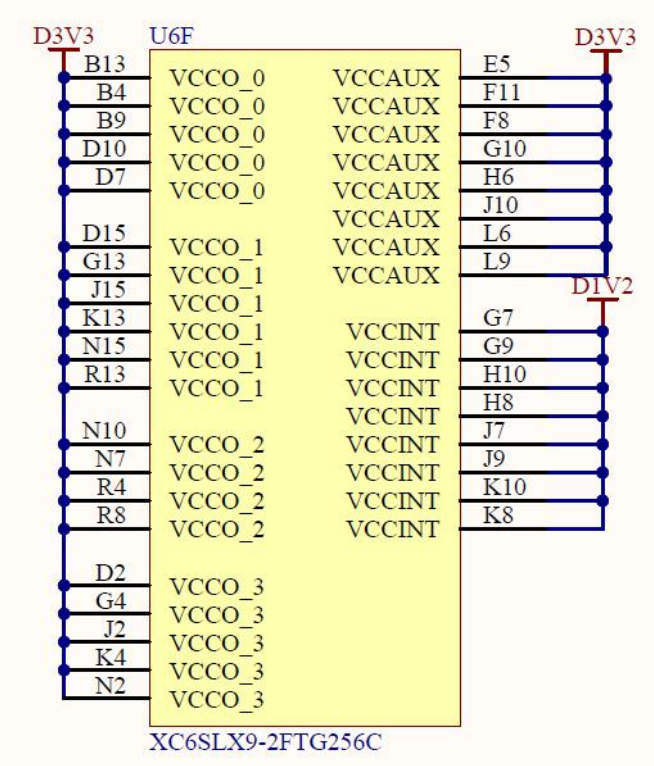


Figure 3-4: FPGA Power Supply

The hardware design of FPGA ground pin is showed as Figure 3-5:

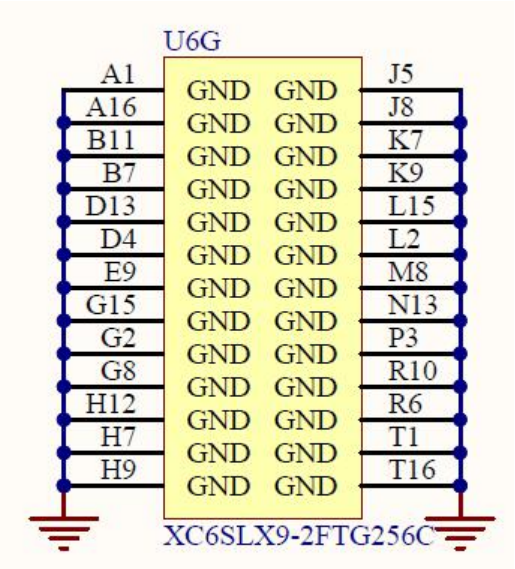


Figure 3-5: FPGA Ground Pin

Part 4: 50Mhz Clock

Figure 4-1 is the clock circuit of the FPGA development board, an 50Mhz crystal oscillator provides the clock source for the whole board. The output of the crystal oscillator is connected to the FPGA T8 Pin (GCLK). This GCLK can be used to drive the user's logic circuit inside the FPGA.

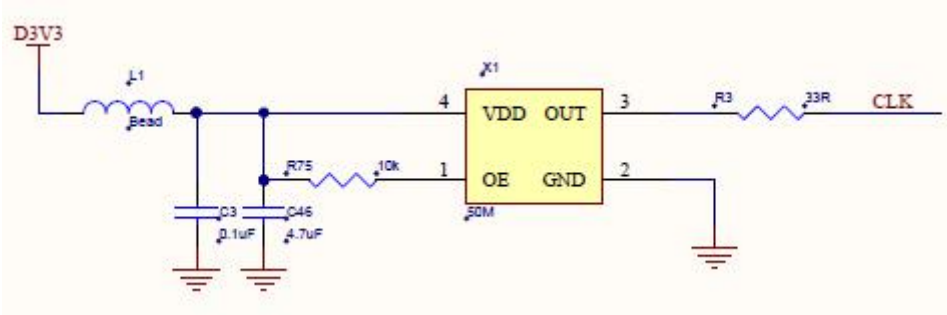


Figure 4-1: 50Mhz Crystal Oscillator

Figure 4-2 shows the onboard 50Mhz crystal oscillator .

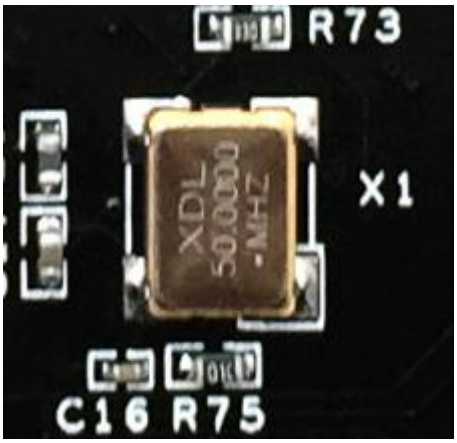


Figure 4-2: 50Mhz crystal oscillator onboard

Net Name	FPGA PIN
CLK	T8

Table 4-1: Clock Pin Assignment

Part 5: SPI Flash

The board uses a 16Mbit SPI FLASH chip, model M25P16, which uses a 3.3V CMOS voltage standard. Due to its non-volatile nature, SPI FLASH can be used as a boot image for FPGA systems in use. These images mainly include FPGA bit files, soft core application code, and other user data files.

The specific models and related parameters of SPI FLASH are shown in Table 5-1

Part	Device	Size	Manufacturer
U8	M25P16	16M bit	ST

Table 5-1: The model of SPI Flash and Parameters

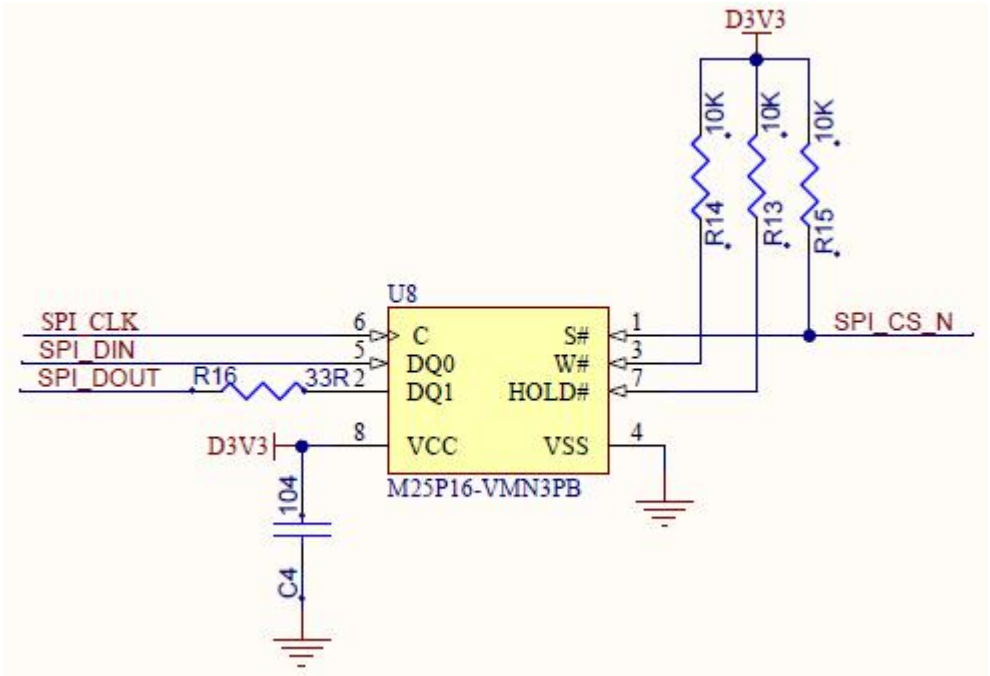


Figure 5-1: The Hardware Design of SPI FLASH

Figure 5-2 shows the onboard SPI FLASH.

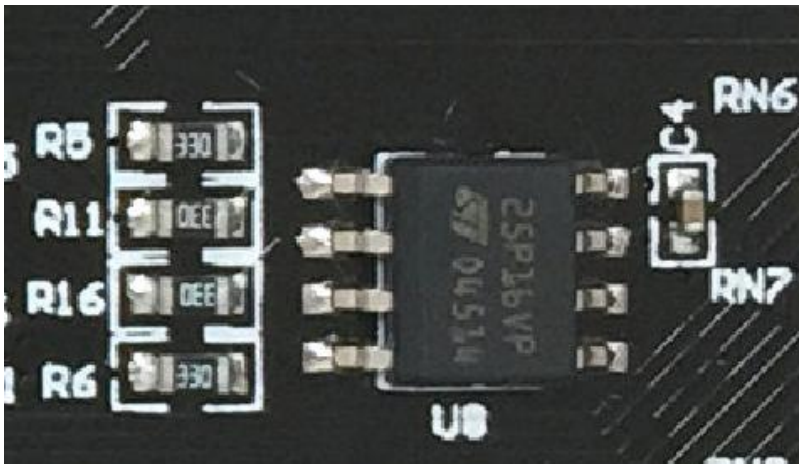


Figure 5-2: SPI Flash Onboard

Pins Assignment of SPI FLASH on Table 5-1

Net Name	FPGA PIN
SPI_CLK	R11
SPI_CS_N	T3
SPI_DIN	T10
SPI_DOUT	P10

Table 5-1: Pin Assignment of SPI FLASH

Part 6: SDRAM

The FPGA development board contains a SDRAM chip, model: HY57V2562GTR, capacity: 256Mbit (16M*16bit), 16bit bus. SDRAM can be used for data caching, such as data collected by the camera module, temporarily stored in SDRAM, and then displayed through the VGA interface. This SDRAM is used for data caching.

Hardware design of SDRAM is showed as Figure 6-1:

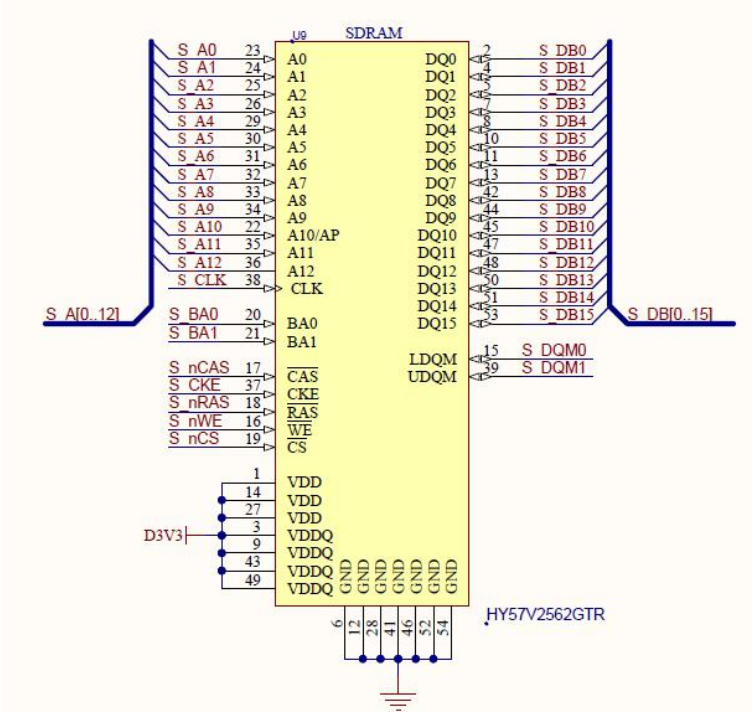


Figure 6-1: SDRAM Hardware Design

Figure 6-2 shows the onboard SDRAM.

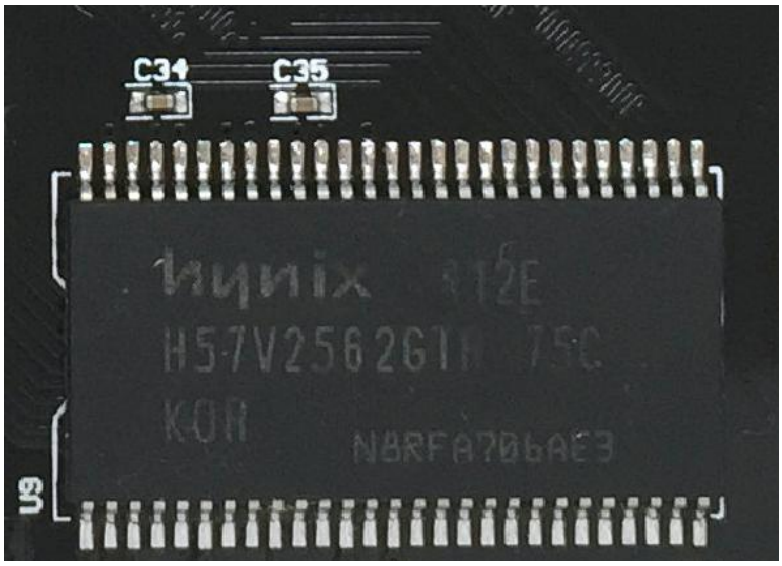


Figure 6-2: SDRAM Onboard

Table 6-1 detailed the PIN Assignment of SDRAM

Net Name	FPGA PIN
S_CLK	H4
S_CKE	H2
S_NCS	G1
S_NWE	E1
S_NCAS	F2
S_NRAS	F1
S_DQM<0>	E2
S_DQM<1>	H1
S_BA<0>	G6
S_BA<1>	J6
S_A<0>	J3
S_A<1>	J4
S_A<2>	K3
S_A<3>	K5
S_A<4>	P1
S_A<5>	N1
S_A<6>	M2
S_A<7>	M1
S_A<8>	L1
S_A<9>	K2
S_A<10>	K6
S_A<11>	K1
S_A<12>	J1
S_DB<0>	A3
S_DB<1>	B3
S_DB<2>	A2
S_DB<3>	B2
S_DB<4>	B1
S_DB<5>	C2
S_DB<6>	C1
S_DB<7>	D1
S_DB<8>	H5

S_DB<9>	G5
S_DB<10>	H3
S_DB<11>	F6
S_DB<12>	G3
S_DB<13>	F5
S_DB<14>	F3
S_DB<15>	F4

Table 6-1: The PIN Assignment of SDRAM

Part 7: EEPROM 24LC04

The development board contains an EEPROM, model 24LC04, and its capacity is 4Kbit (2*256*8bit). It consists of two 256-byte blocks and communicates via the IIC bus. The onboard EEPROM is to learn the communication method of the IIC bus. EEPROM is generally used in the design of instruments and meters, used as a storage of some parameters, power-off is not lost. This chip is simple to operate and has a very high cost performance, so although the capacity ratio is high, the price is very cheap, which is a good choice for those products that are costly.

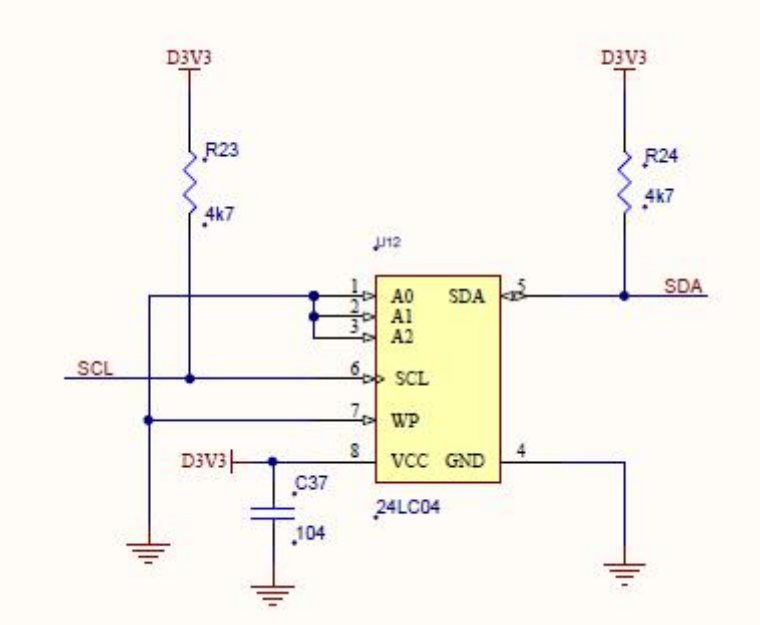


Figure 7-1: EEPROM Design

Figure 7-2 shows the EEPROM on AX309 board：

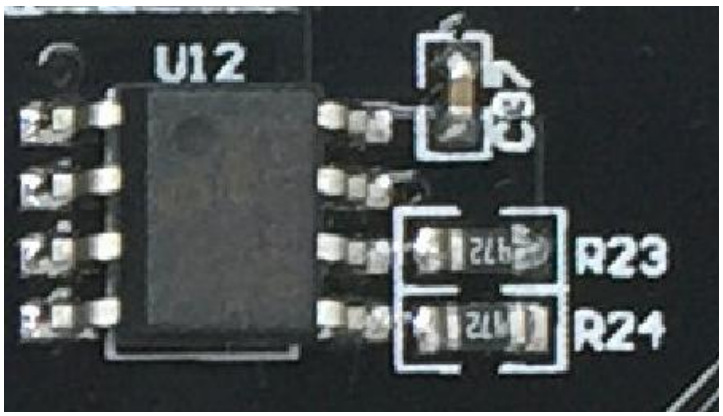


Figure 7-2: EEPROM on AX309 board

Table 7-1 detailed the EEPROM PIN assignment

Net Name	FPGA PIN
SDA	P12
SCL	N12

Table 7-1: EEPROM PIN Assignment

Part 8: RTC

The FPGA development board contains a real-time clock RTC chip, model DS1302. Its function is to provide the calendar function to 2099, with days, minutes, minutes, seconds and weeks. If time is required in the system, the RTC needs to be designed into the product. He needs to connect a 32.768KHz passive clock to provide an accurate clock source to the clock chip, so that the RTC can accurately provide clock information to the product. At the same time, in order to power off the product, the real-time clock can still run normally. Generally, a battery is required to supply power to the clock chip. In Figure 8.1, U7 is the battery holder. We put the button battery (model CR1220, voltage is 3V) into the battery. When the system is powered off, the button battery can also

supply power to the DS1302, so that regardless of whether the product is powered or not, the DS1302 will operate normally without interruption and provide continuous time information. Figure 8.1 shows the schematic of the DS1302

The hardware design of RTC is showed as Figure 8-1:

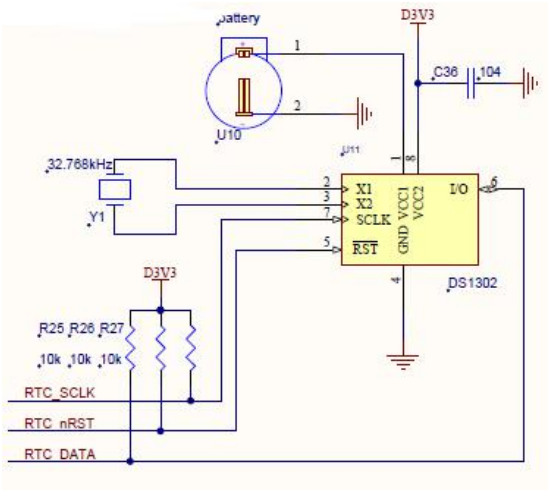


Figure 8-1: RTC Hardware Design

Figure 8-2 shows the DS1302 circuit on AX309 board.

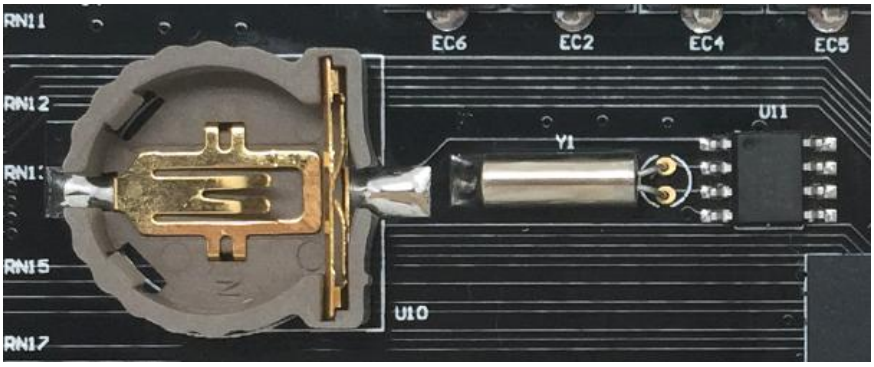


Figure 8-2: DS1302 Circuit Onboard

Table 8-1 detailed the DS1302 Pin Assignment：

Net Name	FPGA PIN
RTC_SCIK	E13
RTC_nRST	C13
RTC_DATA	D14

Table 8-1: The DS1302 Pin Assignment

Part 9: USB Serial Port

The development board contains the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface uses the MINI USB interface. The USB interface can implement the power supply function, and the USB to serial port function can be realized. It can be connected to the USB port of the PC for serial data communication by using a USB cable.

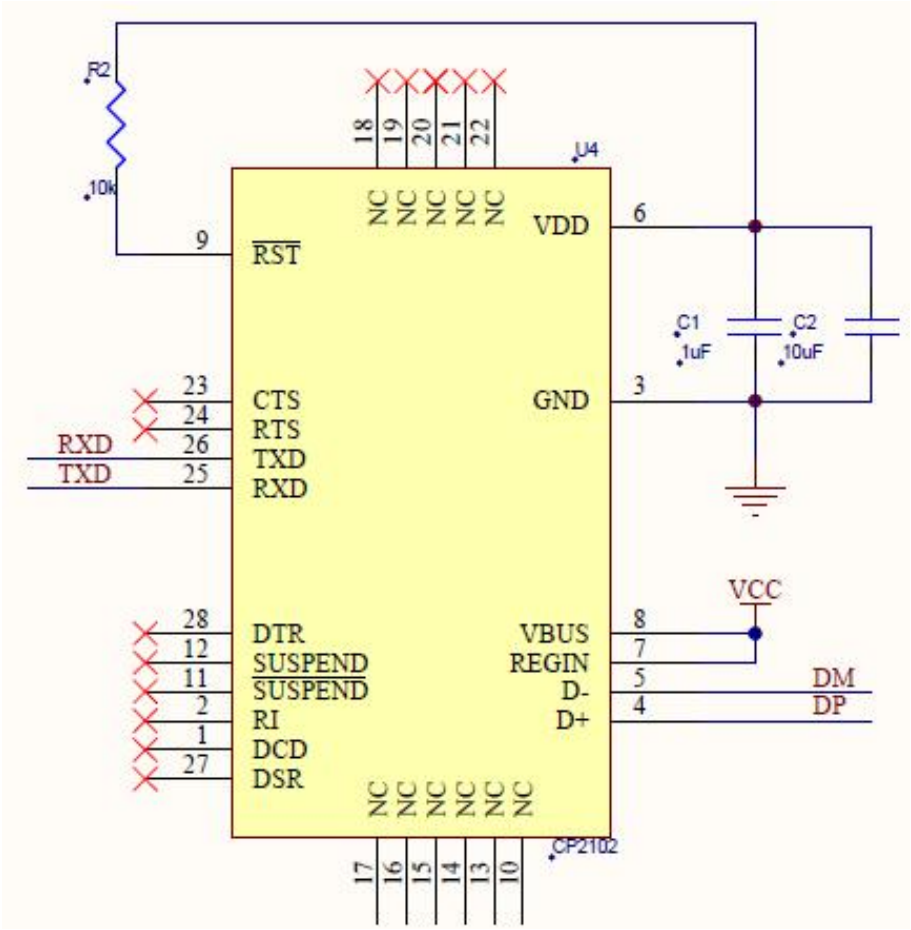


Figure 9-1: USB UART Interface

Figure 9-2 shows the USB UART onboard.

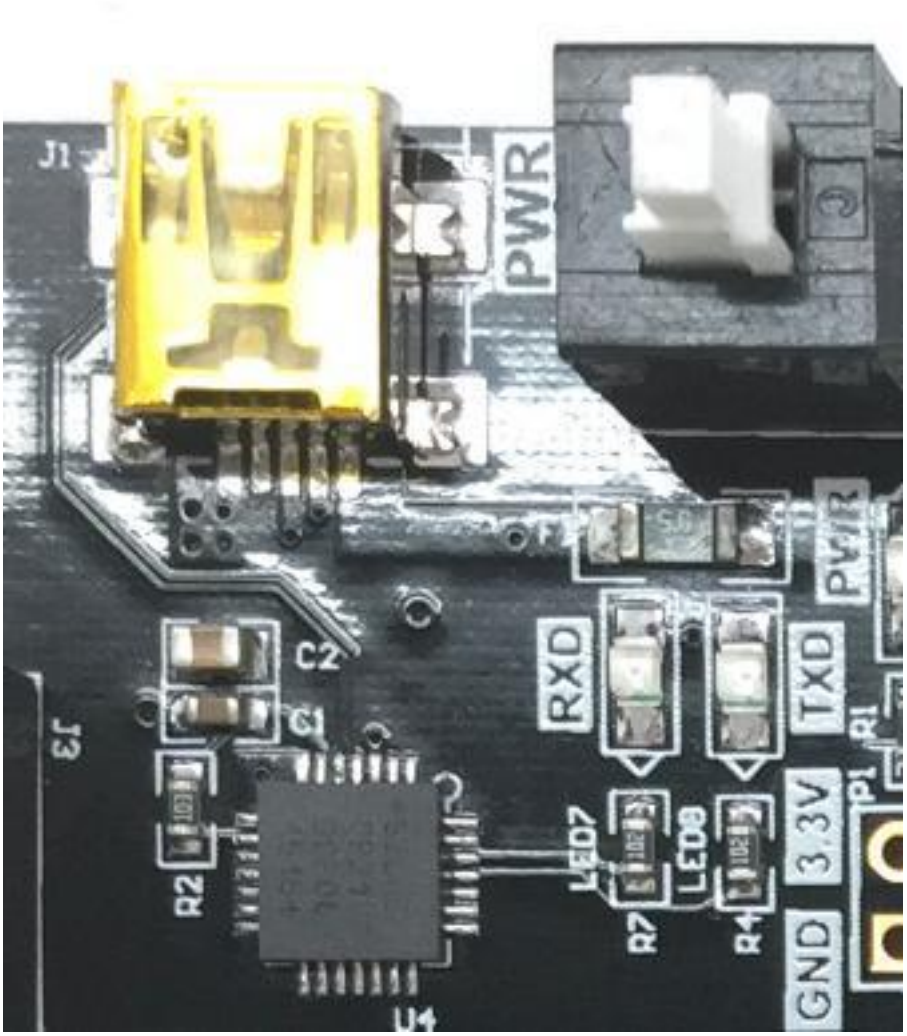


Figure 9-2: USB UART Onboard

There are two LEDs on board to indicate the UART operation status, the RXD LED is used to indicate receiving status, and the TXD LED is used to indicate send status. The indication LEDs is design as Figure 9-3.

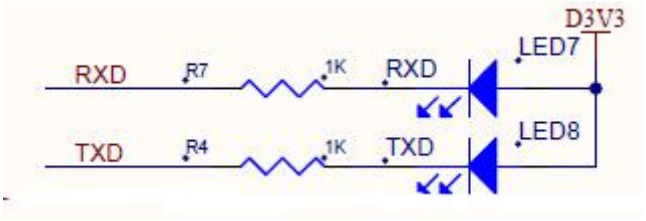


Figure 9-3: USB UART LED Indication

Table 9-1 detailed the PIN Assignment of USB Uart:

Net Name	FPGA PIN
RXD	C11
TXD	D12

Table 9-1: The PIN Assignment of USB Uart

Part 10: VGA Port

VGA interface, I believe many friends will not be unfamiliar, because this interface is the most important interface on the computer monitor. From the era of huge CRT monitors, the VGA interface has been used, and it has been used until now, and the VGA interface is also called For the D-Sub interface.

The VGA connector is a D-type connector with a total of 15 pinholes divided into three rows of five. More important are the three RGB color component signals and the two scan sync signals HSYNC and VSYNC pins.

Pins 1, 2, and 3 are red, green, and blue primary color analog voltages, which are 0 to 0.714V peak-peak, 0V is colorless, and 0.714V is full color. Some non-standard displays use a full color level of 1Vpp.

The three primary color source terminals and terminal matching resistors are both 75 ohms, detailed as Figure 10-1

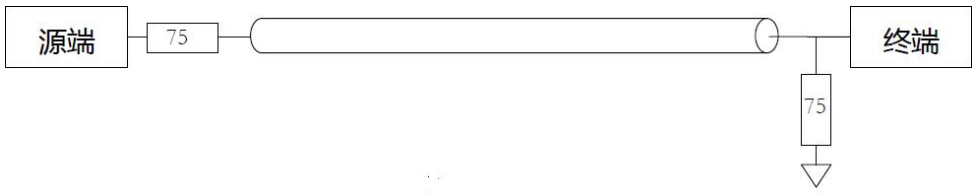


Figure 10-1: VGA video signal transmission diagram

HSYNC and VSYNC are line data synchronization and frame data synchronization, respectively, which are TTL levels. The FPGA can only output

digital signals, while the R, G, and B required by VGA are analog signals. The digital to analog signal of VGA is realized by a simple resistor circuit. This resistor circuit can generate 32 gradient grade red and blue signals and 64 gradient grade green signals (RGB 5-6-5). Figure 10-2 detailed the VGA interface hardware design.

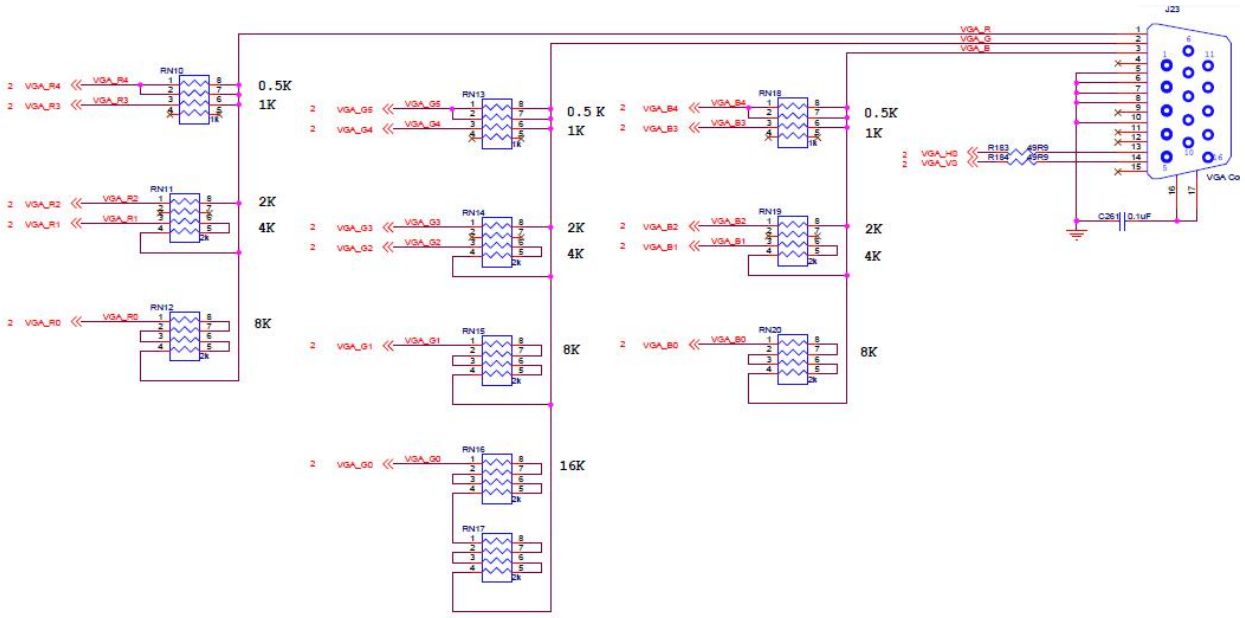


Figure 10-2: VGA Interface Hardware Design

Figure 10-3 shows the VGA interface onboard.

Figure 10-3: VGA Interface Onboard

Table 10-1 detailed the Pin Assignment of VGA Interface.

Net Name	FPGA PIN	Remark
VGA_D<0>	P7	BLUE<0>

VGA_D<1>	M7	BLUE<1>
VGA_D<2>	P8	BLUE<2>
VGA_D<3>	N8	BLUE<3>
VGA_D<4>	L7	BLUE<4>
VGA_D<5>	M9	GREEN<0>
VGA_D<6>	N9	GREEN<1>
VGA_D<7>	P9	GREEN<2>
VGA_D<8>	L10	GREEN<3>
VGA_D<9>	M10	GREEN<4>
VGA_D<10>	P11	GREEN<5>
VGA_D<11>	M11	RED<0>
VGA_D<12>	M12	RED<1>
VGA_D<13>	L12	RED<2>
VGA_D<14>	N14	RED<3>
VGA_D<15>	M13	RED<4>
VGA_HS	M14	Horizontal sync signal
VGA_VS	L13	Vertical sync signal

Table 10-1: The Pin Assignment of VGA Interface

Part 11: SD Card Slot

The SD card (Secure Digital Memory Card) is a memory card based on the semiconductor flash memory process. It was completed in 1999 by the Japanese Panasonic-led concept, and the participants Toshiba and SanDisk of the United States conducted substantial research and development. In 2000, these companies initiated the establishment of the SD Association (Secure Digital Association, SDA), which has a strong lineup and attracted a large number of manufacturers. These include IBM, Microsoft, Motorola, NEC, Samsung, and others. Driven by these leading manufacturers, SD cards have become the most widely used memory card in consumer digital devices.

SD card is a very popular storage device now, in AX309 board a Micro SD socket is designed for SD card access. FPGA uses the SPI interface to read or

write the SD card in AX309. The hardware design of SD socket is showed as Figure 11-1.

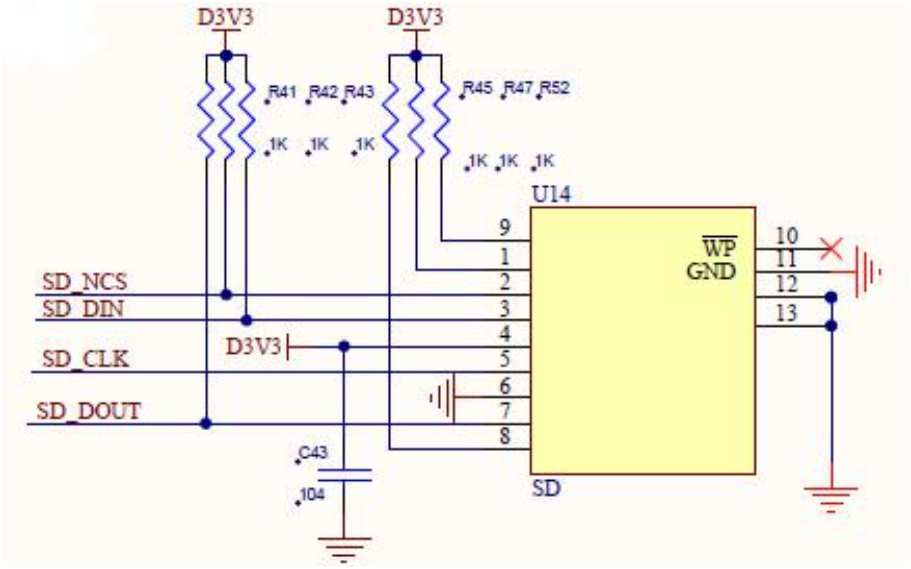


Figure 11-1: SD Socket Design

Figure 11-2 is the SD socket onboard.

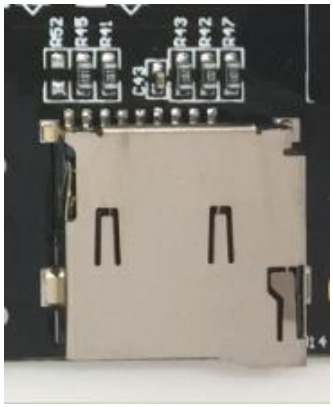


Figure 11-2: SD Socket Onboard

Table 11-1 detailed Pin Assignment of SD Socket.

SPI Mode	
Net Name	FPGA PIN
SD_NCS	N3
SD_DIN	L5
SD_CLK	M3
SD_DOUT	L4

Table 11-1: The Pin Assignment of SD Socket

Part 12: LED

The FPGA development board contains four user LEDs. The schematic of the four user LED sections is shown in Figure 12-1. When the FPGA pin output is logic 0, the LED will go out. When the output is logic 1, the LED is illuminated.

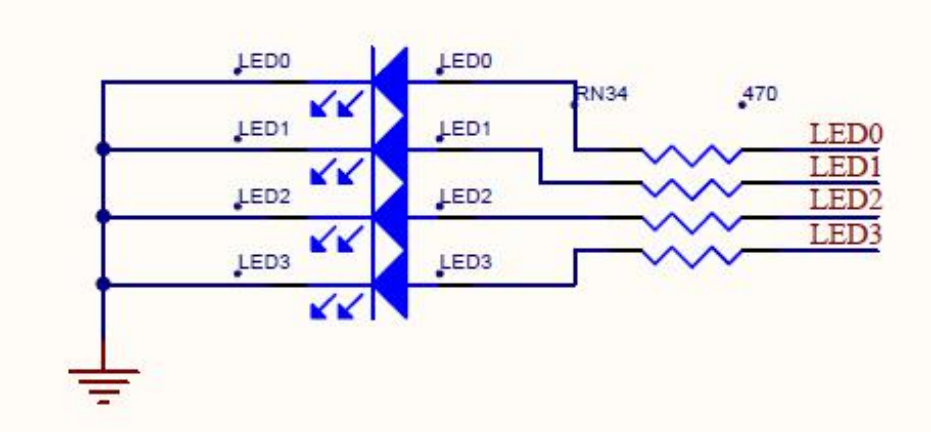


Figure 12-1: LEDs Design

Figure 12-2 is the LEDs onboard.

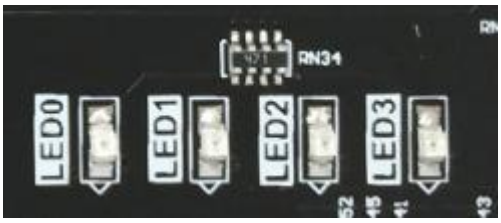


Figure 12-2: 4 LEDs Onboard

Table 12-1 detailed the Pin Assignment of LEDs：

Net Name	FPGA PIN
LED<0>	P4
LED<1>	N5
LED<2>	P5
LED<3>	M6

Table 12-1: The Pin Assignment of LEDs

Part 13: Buttons

The board has six buttons, it includes four user buttons (KEY1~KEY4) and two special buttons (PROG and RESET). These six buttons are active low when pressed. The hardware design of the four user keys is shown in Figure 13-1

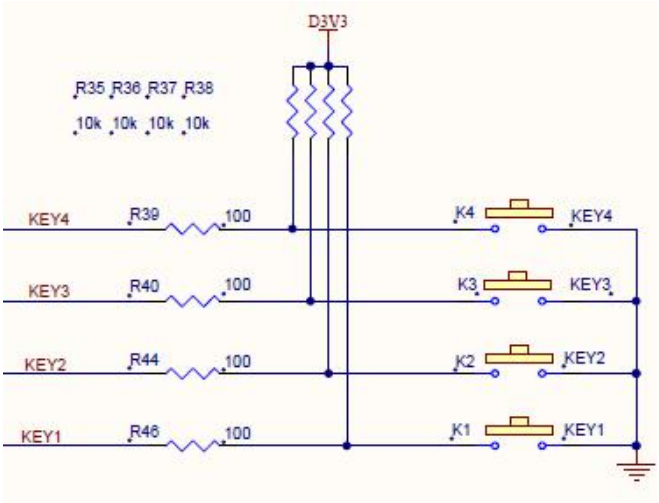


Figure 13-1: Design of User Buttons

There are two buttons for special function, one is for RESET function and another is for CONFIG function. The RESET button is connected to FPGA IO and the CONFIG button is connected to PROGRAM pin of FPGA. The hardware design of these two special buttons is shown in Figure 13-2

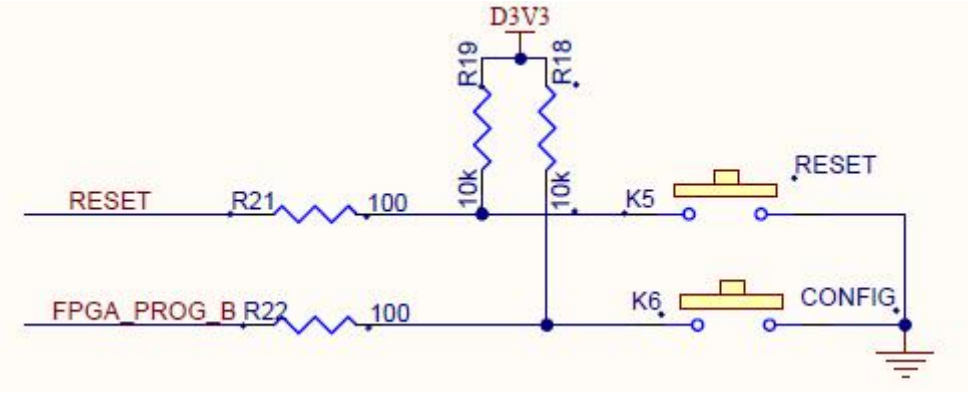


Figure 13-2: Design of Special Buttons

Figure 13-3 is the six buttons onboard.

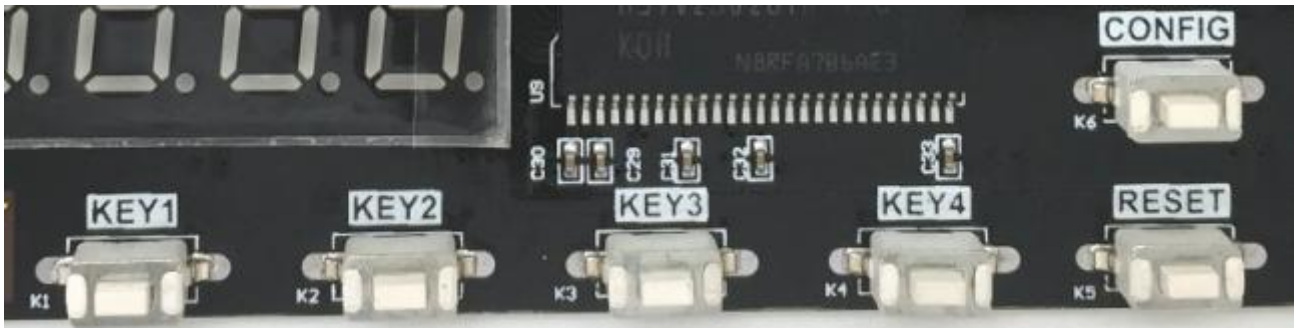


Figure 13-3: Six Button Onboard

Table 13-1 detailed the Pin Assignment of Buttons.

Net Name	FPGA PIN
KEY1	C3
KEY2	D3
KEY3	E4
KEY4	E3
RESET	L3
PROG	T2

Table 13-1: The Pin Assignment of Buttons

Part 14: Camera Port

The development board includes an 18-pin CMOS camera interface that can be connected to the OV7670 camera module and the OV5640 camera module to enable video capture. After acquisition, the display can be connected via a TFT LCD module or a VGA interface. OV7670, 30W pixels, output resolution is 640 * 480; OV5640, 500W pixels, output resolution up to 2592 * 1944. Regarding camera selection, users can purchase according to their actual needs. The CMOS camera interface is designed as Figure 14-1:

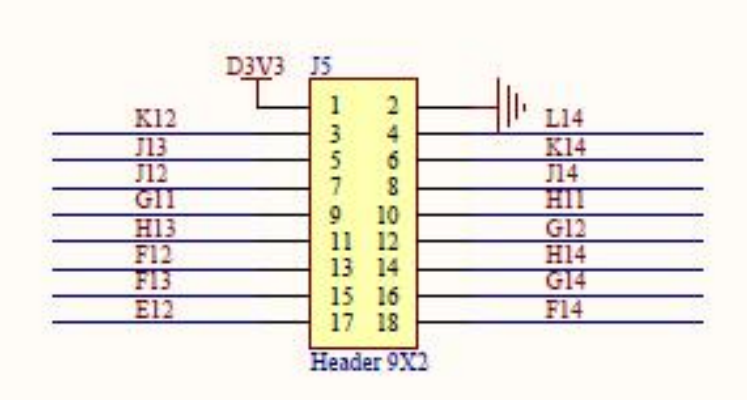


Figure 14-1: CMOS Camera interface

The Camera interface is showed as Figure 14-2 (OV5640 Camera Module is required be purchase separately）

Figure 14-2: Camera Interface with OV5640 Module

Table 14-1 detailed Pin Assignment of CMOS Camera Interface.

J5	Net Name	FPGA 引脚
3	CMOS_SCLK	K12
4	CMOS_SDAT	L14
5	CMOS_VSYNC	J13
6	CMOS_HREF	K14
7	CMOS_PCLK	J12
8	CMOS_XCLK	J14

9	CMOS_D<7>	G11
10	CMOS_D<6>	H11
11	CMOS_D<5>	H13
12	CMOS_D<4>	G12
13	CMOS_D<3>	F12
14	CMOS_D<2>	H14
15	CMOS_D<1>	F13
16	CMOS_D<0>	G14
17	CMOS_RESET	E12
18	CMOS_PWDN	F14

Table 14-1: The Pin Assignment of CMOS Camera Interface

Part 15: 7-segment displays

The digital tube is a very common display device. It is generally divided into a seven-segment digital tube and an eight-segment digital tube. The difference between the two is that the eight-segment digital tube has a more "point" than the seven-segment digital tube. The digital tube we use is a 6-in-one eight-segment digital tube. The segment structure of the digital tube is shown in Figure 15-1.

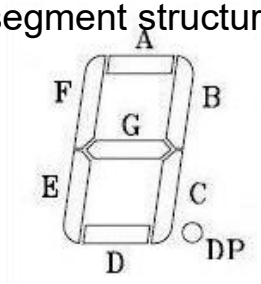


Figure 15-1: Segment Structure of Digital Tube

The FPGA Development Board use a common anode digital tube. When the corresponding pin of a field is low, the corresponding field is lit. When the corresponding pin of a certain field is high, the corresponding field is not lit.

After the above schematic, let's look at the design on the FPGA development board AX309.

The six-in-one digital tube is a dynamic display. Due to the persistence of

human vision and the afterglow effect of the LED, although the digital tubes are not lit at the same time, as long as the scanning speed is fast enough, the impression is a group. stable display data, no flickering.

The same segments of the six-in-one digital tube are connected together, a total of 8 pins, and then add 6 control signal pins, a total of 14 pins, as shown in Figure 15-2, where DIG[0. .7] is the corresponding digital tube A, B, C, D, E, F, G, H (ie point DP); SEL [0..5] is the six control pins of the six digital tube, is also low level is active. When the control pin is low, the corresponding digital tube has a power supply voltage, so that the digital tube can be lit. Otherwise, no matter how the segment of the digital tube changes, the corresponding digital tube cannot be lit.

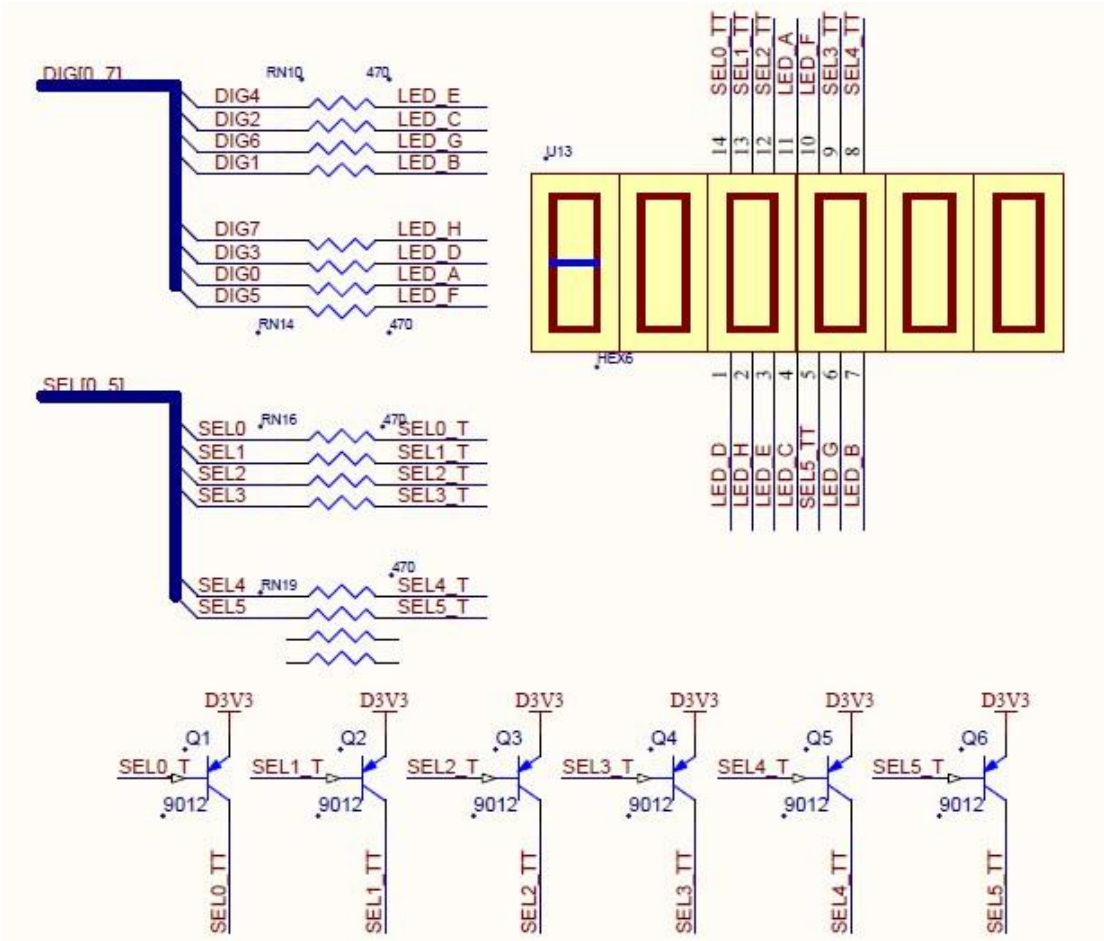


Figure 15-2: Hardware Design of Seven Segments

Figure 15-3 is the Seven Segments on board

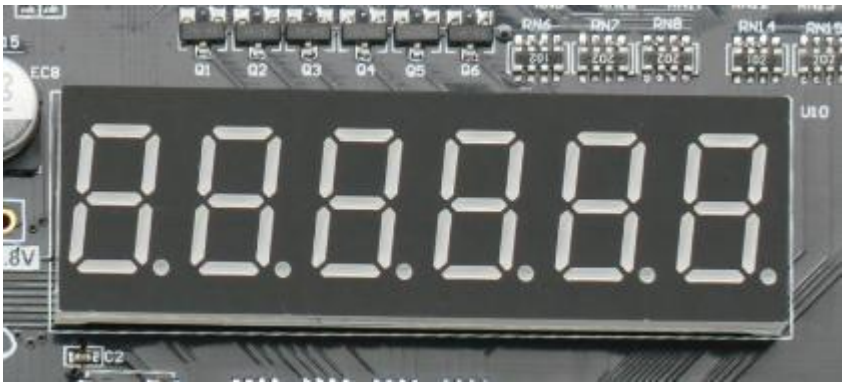


Figure 15-3: Seven Segments on board

Table 15-1 detailed the pin assignment of FPGA to the 7-segment displays.

Net Name	FPGA PIN	Description
DIG[0]	C7	Segment Digit A
DIG[1]	E6	Segment Digit B
DIG[2]	C5	Segment Digit C
DIG[3]	F7	Segment Digit D
DIG[4]	D6	Segment Digit E
DIG[5]	E7	Segment Digit F
DIG[6]	D5	Segment Digit G
DIG[7]	C6	Segment Digit DP
SEL[0]	D8	#1 Segments Select
SEL[1]	E8	#2 Segments Select
SEL[2]	F9	#3 Segments Select
SEL[3]	F10	#4 Segments Select
SEL[4]	E10	#5 Segments Select
SEL[5]	D9	#6 Segments Select

Table 15-1: The Pin Assignment of the FPGA

Part 16: Buzzer

The board has one buzzer which is mainly used for prompt or alarm. the buzzer is controlled by a transistor, when FPGA output a low signal, the buzzer

will on and sound, when FPGA output a high signal, the buzzer will off. For the sake of convenience, we have added a jump cap (CB1) between the buzzer and the FPGA. If you hate the buzzer, you can remove the jumper. The hardware design of buzzer is showed as Figure 16-1:

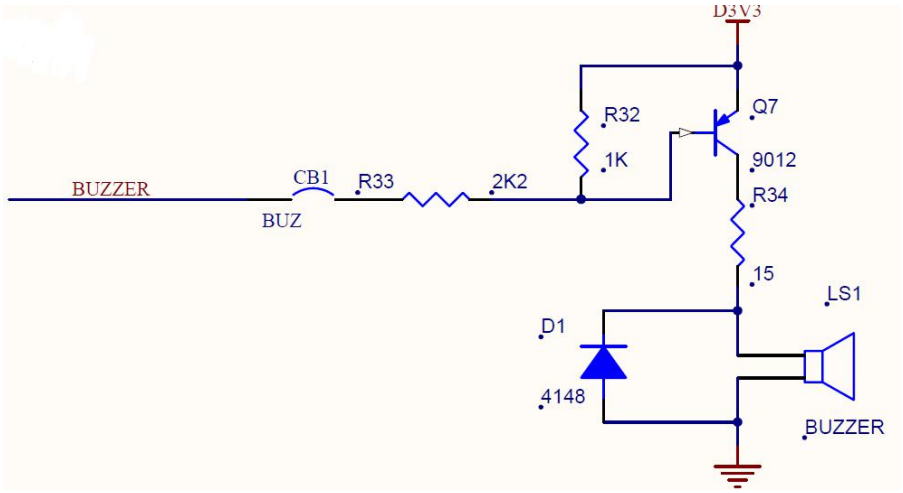


Figure 16-1: Hardware Design of buzzer

Figure 16-2 is showed the buzzer onboard, we can disable the buzzer by removing the jumper cap of CB1.

Figure 16-2: Buzzer Onboard

Table 16-1 detailed the Pin Assignment of Buzzer：

Net Name	FPGA PIN
BUZZER	J11

Table 16-1: The Pin Assignment of Buzzer

Part 17: GPIO Expansion Headers

The development board reserves 2 expansion ports, and the expansion port has 40 signals, of which 5V power supply 1 way, 3.3V power supply 2 way, ground 3 way, IO port 34 way. These IO ports are independent IO ports and are not multiplexed with other devices. The IO port is connected to the FPGA pin at a level of 3.3V. Do not connect directly to a 5V device to avoid burning the FPGA. If you want to connect a 5V device, you need to connect a level shifting chip.

The FPGA IO pins on the expansion headers are connected to a 33ohm resistor for protection against high or low voltage level. Figure 17-1 and Figure 17-2 shows the connection circuitry of these two 40-pin expansion headers.

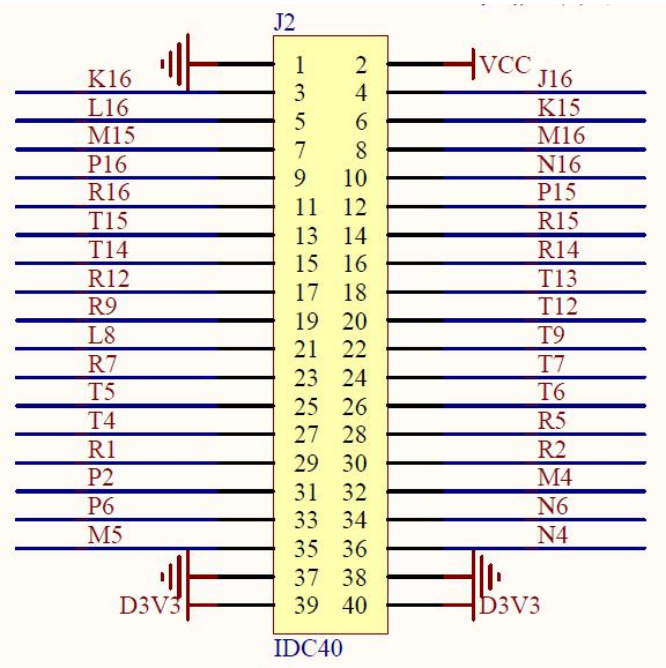


Figure 17-1: J2 Expansion Headers

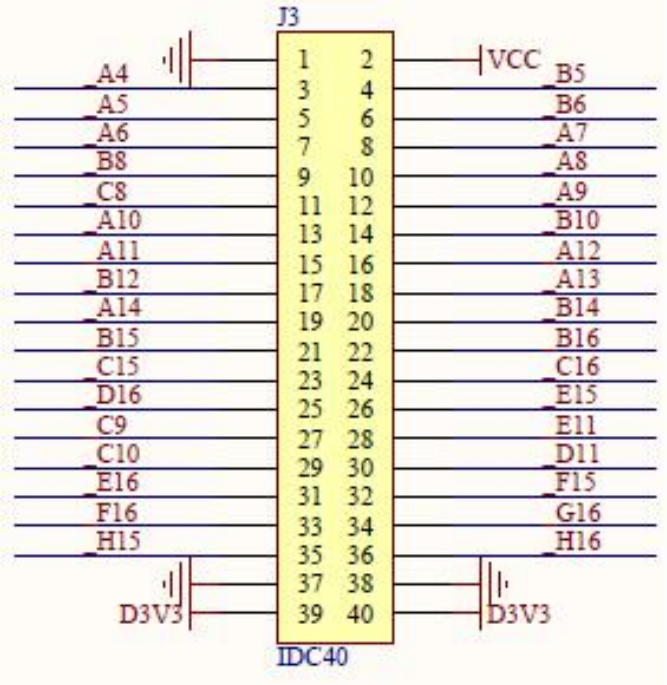


Figure 17-3: J3 Expansion Headers

Figure 17-3 is the header of J2 and J3 on AX309 board, the Pin1, Pin2 and Pin39 , Pin40 of connector are marked on PCB board.

Figure 17-3: J2, J3 Connector Onboard

Expansion Header of AX309 can use to connect ALINX module to expand

the additional function, for example connect to LCD module or ADDA module. When the expansion port is connected to the expansion module, the direction is as shown in Figure 17-4, and the pins 1 and 2 are above the interface (note the identification on the PCB).

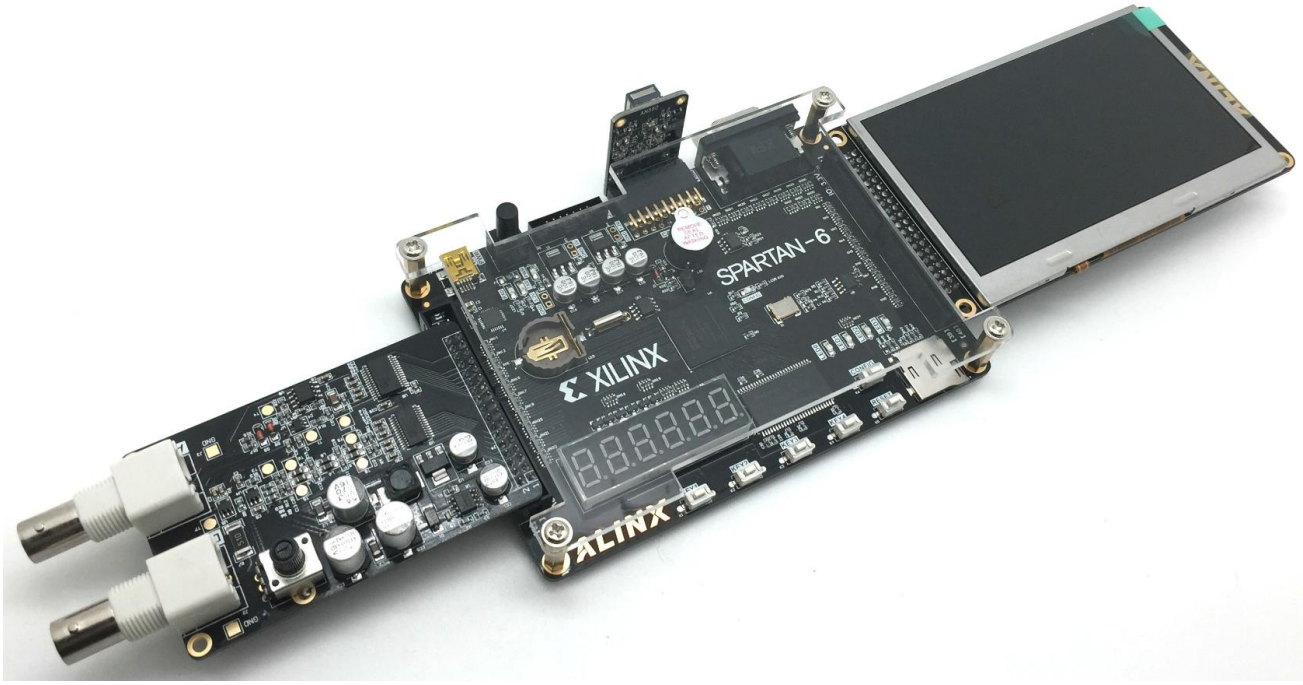


Figure 17-4: Header Connection

Table 17-1 detailed the Pin Assignment of J2.

J2 PIN	FPGA PIN	J2 PIN	FPGA PIN
1	GND	**2**	VCC5V
3	K16	**4**	J16
5	L16	**6**	K15
7	M15	**8**	M16
9	P16	**10**	N16
11	R16	**12**	P15
13	T15	**14**	R15
15	T14	**16**	R14
17	R12	**18**	T13
19	R9	**20**	T12
21	L8	**22**	T9
23	R7	**24**	T7

25	T5	**26**	T6
27	T4	**28**	R5
29	R1	**30**	R2
31	P2	**32**	M4
33	P6	**34**	N6
35	M5	**36**	N4
37	GND	**38**	GND
39	D3V3	**40**	D3V3

Table 17-1: The Pin Assignment of J2.

Table 17-2 detailed the Pin Assignment of J3

J3 PIN	FPGA PIN	J3 PIN	FPGA PIN
1	GND	**2**	VCC5V
3	A4	**4**	B5
5	A5	**6**	B6
7	A6	**8**	A7
9	B8	**10**	A8
11	C8	**12**	A9
13	A10	**14**	B10
15	A11	**16**	A12
17	B12	**18**	A13
19	A14	**20**	B14
21	B15	**22**	B16
23	C15	**24**	C16
25	D16	**26**	E15
27	C9	**28**	E11
29	C10	**30**	D11
31	E16	**32**	F15
33	F16	**34**	G16
35	H15	**36**	H16
37	GND	**38**	GND
39	D3V3	**40**	D3V3

Table 17-2: The Pin Assignment of J2.