



# TN12, TS12 and TYNx12 Series

SENSITIVE & STANDARD

12A SCRs

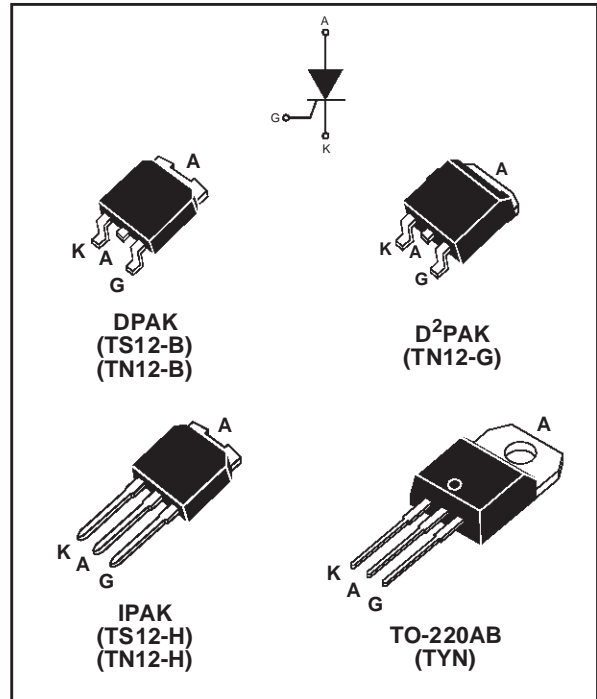
## MAIN FEATURES:

Symbol	Value	Unit
$I_{T(RMS)}$	12	A
$V_{DRM}/V_{RRM}$	600 to 1000	V
$I_{GT}$	0.2 to 15	mA

## DESCRIPTION

Available either in sensitive (TS12) or standard (TYN, TN12...) gate triggering levels, the 12A SCR series is suitable to fit all modes of control found in applications such as overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, in-rush current limiting circuits, capacitive discharge ignition, voltage regulation circuits...

Available in through-hole or surface-mount packages, they provide an optimized performance in a limited space area.



## ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit	
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)		$T_c = 105^\circ\text{C}$ 12	A	
$I_{T(AV)}$	Average on-state current (180° conduction angle)		$T_c = 105^\circ\text{C}$ 8	A	
$I_{TSM}$	Non repetitive surge peak on-state current	$t_p = 8.3 \text{ ms}$	$T_j = 25^\circ\text{C}$ 115	A	
		$t_p = 10 \text{ ms}$			146
$I_t$	$I_t$ Value for fusing	$t_p = 10 \text{ ms}$	$T_j = 25^\circ\text{C}$ 60	98	A s
$di/dt$	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$ , $t_r \leq 100 \text{ ns}$	$F = 60 \text{ Hz}$	$T_j = 125^\circ\text{C}$ 50		A/ $\mu\text{s}$
$I_{GM}$	Peak gate current	$t_p = 20 \mu\text{s}$	$T_j = 125^\circ\text{C}$ 4		A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125^\circ\text{C}$ 1		W
$T_{stg}$ $T_j$	Storage junction temperature range Operating junction temperature range		- 40 to + 150 - 40 to + 125		$^\circ\text{C}$
$V_{RGM}$	Maximum peak reverse gate voltage (for TN12 & TYN)		5		V

## TN12, TS12 and TYNx12 Series

### ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C, unless otherwise specified)

#### ■ SENSITIVE

Symbol	Test Conditions		TS1220	Unit	
I <sub>GT</sub>	V <sub>D</sub> = 12 V    R <sub>L</sub> = 140 Ω	MAX.	200	μA	
V <sub>GT</sub>		MAX.	0.8	V	
V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> R <sub>L</sub> = 3.3 kΩ    R <sub>GK</sub> = 1 kΩ    T <sub>j</sub> = 125°C	MIN.	0.1	V	
V <sub>RG</sub>	I <sub>RG</sub> = 10 μA	MIN.	8	V	
I <sub>H</sub>	I <sub>T</sub> = 50 mA    R <sub>GK</sub> = 1 kΩ	MAX.	5	mA	
I <sub>L</sub>	I <sub>G</sub> = 1 mA    R <sub>GK</sub> = 1 kΩ	MAX.	6	mA	
dV/dt	V <sub>D</sub> = 67 % V <sub>DRM</sub> R <sub>GK</sub> = 220 Ω    T <sub>j</sub> = 125°C	MIN.	5	V/μs	
V <sub>TM</sub>	I <sub>TM</sub> = 24 A    t <sub>p</sub> = 380 μs    T <sub>j</sub> = 25°C	MAX.	1.6	V	
V <sub>t0</sub>	Threshold voltage    T <sub>j</sub> = 125°C	MAX.	0.85	V	
R <sub>d</sub>	Dynamic resistance    T <sub>j</sub> = 125°C	MAX.	30	mΩ	
I <sub>DRM</sub> I <sub>RRM</sub>	V <sub>DRM</sub> = V <sub>RRM</sub> R <sub>GK</sub> = 220 Ω	T <sub>j</sub> = 25°C	MAX.	5	μA
		T <sub>j</sub> = 125°C		2	mA

#### ■ STANDARD

Symbol	Test Conditions	TN1215		TYN		Unit	
		B/H	G	x12T	x12		
I <sub>GT</sub>	V <sub>D</sub> = 12 V    R <sub>L</sub> = 33 Ω	MIN.	2	0.5	2	mA	
		MAX.	15	5	15		
V <sub>GT</sub>		MAX.	1.3			V	
V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> R <sub>L</sub> = 3.3 kΩ    T <sub>j</sub> = 125°C	MIN.	0.2			V	
I <sub>H</sub>	I <sub>T</sub> = 500 mA    Gate open	MAX.	40	30	15	30	mA
I <sub>L</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>	MAX.	80	60	30	60	mA
dV/dt	V <sub>D</sub> = 67 % V <sub>DRM</sub> Gate open    T <sub>j</sub> = 125°C	MIN.	200		40	200	V/μs
V <sub>TM</sub>	I <sub>TM</sub> = 24 A    t <sub>p</sub> = 380 μs    T <sub>j</sub> = 25°C	MAX.	1.6				V
V <sub>t0</sub>	Threshold voltage    T <sub>j</sub> = 125°C	MAX.	0.85				V
R <sub>d</sub>	Dynamic resistance    T <sub>j</sub> = 125°C	MAX.	30				mΩ
I <sub>DRM</sub> I <sub>RRM</sub>	V <sub>DRM</sub> = V <sub>RRM</sub>	T <sub>j</sub> = 25°C	MAX.		5		μA
		T <sub>j</sub> = 125°C			2		mA

### THERMAL RESISTANCES

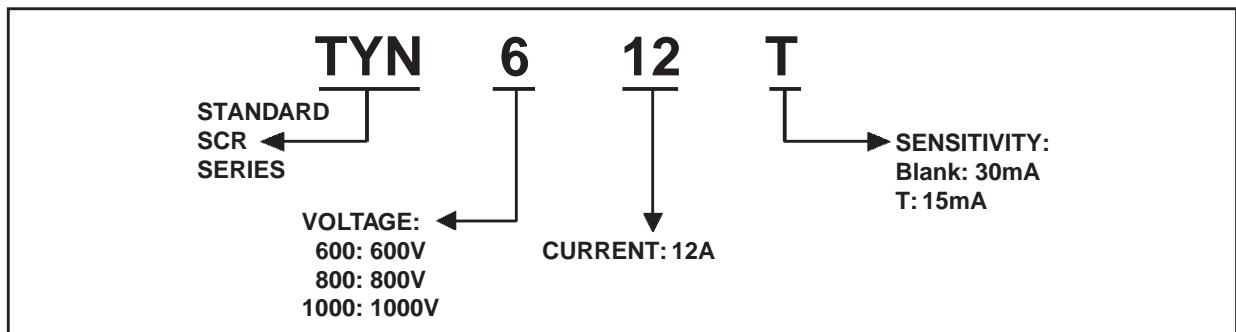
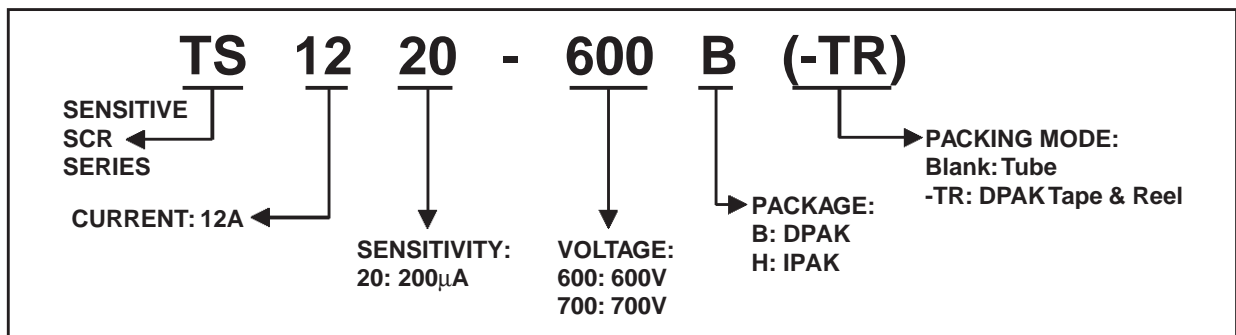
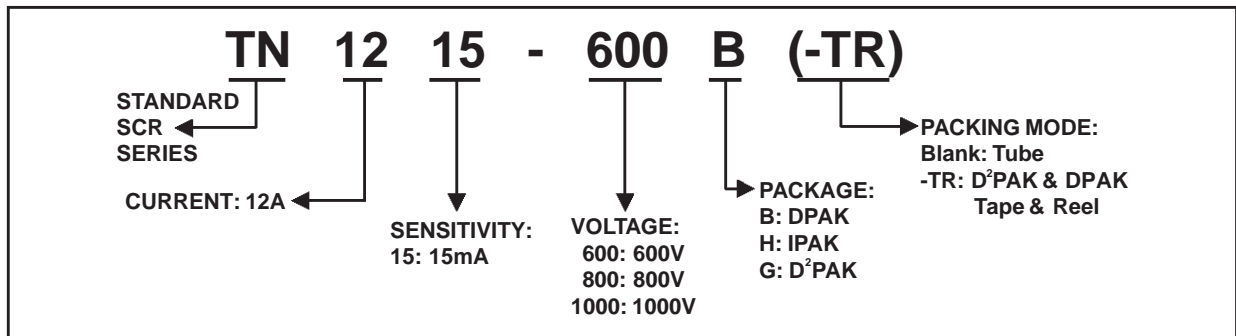
Symbol	Parameter	Value	Unit	
R <sub>th(j-c)</sub>	Junction to case (DC)	1.3	°C/W	
R <sub>th(j-a)</sub>	Junction to ambient	TO-220AB	60	°C/W
		I <sub>PAK</sub>	100	
	S = 1 cm	D PAK	45	
	S = 0.5 cm	DPAK	70	

S = Copper surface under tab

PRODUCT SELECTOR

Part Number	Voltage (xxx)				Sensitivity	Package
	600 V	700 V	800 V	1000 V		
TN1215-xxxB	X		X		15 mA	DPAK
TN1215-xxxG	X		X	X	15 mA	D PAK
TN1215-xxxH	X		X		15 mA	IPAK
TS1220-xxxB	X	X			0.2 mA	DPAK
TS1220-xxxH	X	X			0.2 mA	IPAK
TYNx12	X		X	X	30 mA	TO-220AB
TYNx12T	X		X	X	15 mA	TO-220AB

ORDERING INFORMATION



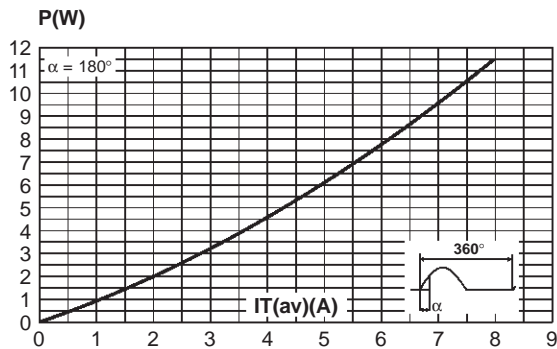
# TN12, TS12 and TYNx12 Series

## OTHER INFORMATION

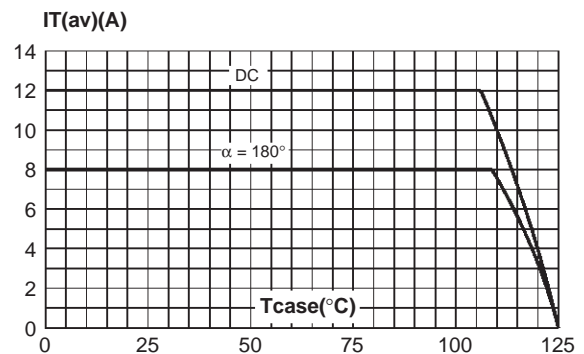
Part Number	Marking	Weight	Base Quantity	Packing mode
TN1215-x00B	TS1215x00	0.3 g	75	Tube
TN1215-x00B-TR	TS1215x00	0.3 g	2500	Tape & reel
TN1215-x00G	TS1215x00G	1.5 g	50	Tube
TN1215-x00G-TR	TS1215x00G	1.5 g	1000	Tape & reel
TN1215-x00H	TN1215x00	0.4 g	75	Tube
TS1220-x00B	TS1220x00	0.3 g	75	Tube
TS1220-x00B-TR	TS1220x00	0.3 g	2500	Tape & reel
TS1220-x00H	TS1220x00	0.4 g	75	Tube
TYNx12	TYNx12	2.3 g	250	Bulk
TYNx12RG	TYNx12	2.3 g	50	Tube
TYNx12T	TYNx12T	2.3 g	250	Bulk
TYNx12TRG	TYNx12T	2.3 g	50	Tube

Note: x = voltage

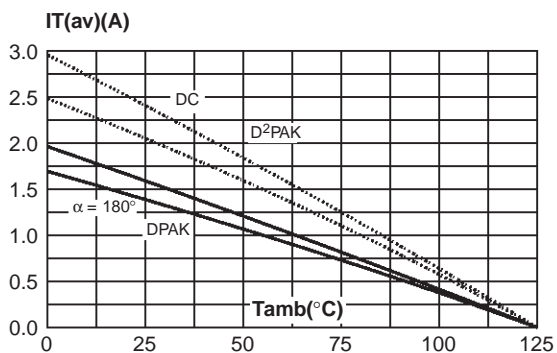
**Fig. 1:** Maximum average power dissipation versus average on-state current.



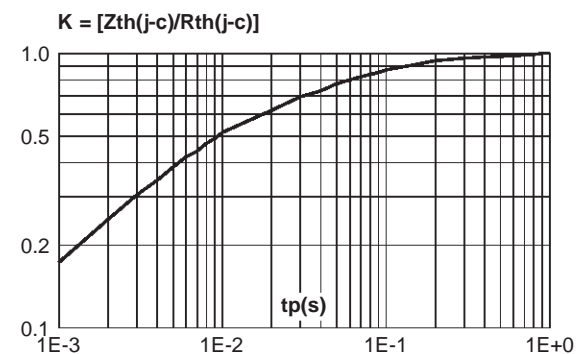
**Fig. 2-1:** Average and D.C. on-state current versus case temperature.



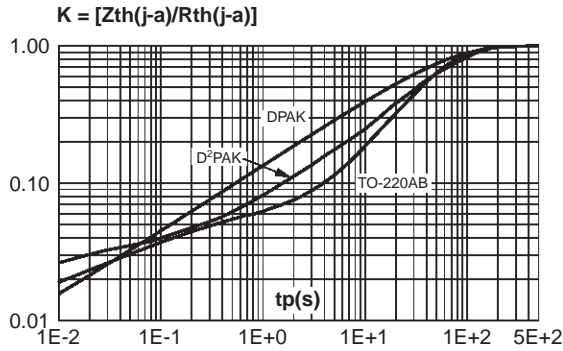
**Fig. 2-2:** Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout) (DPAK and D<sup>2</sup>PAK).



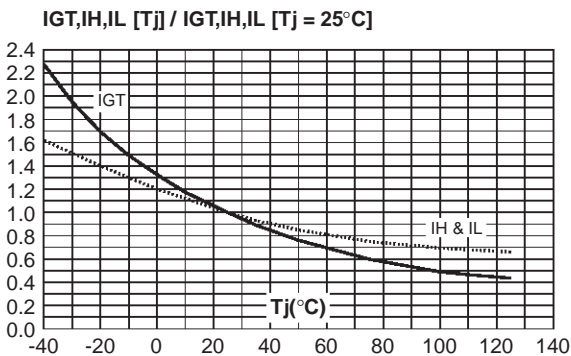
**Fig. 3-1:** Relative variation of thermal impedance junction to case versus pulse duration.



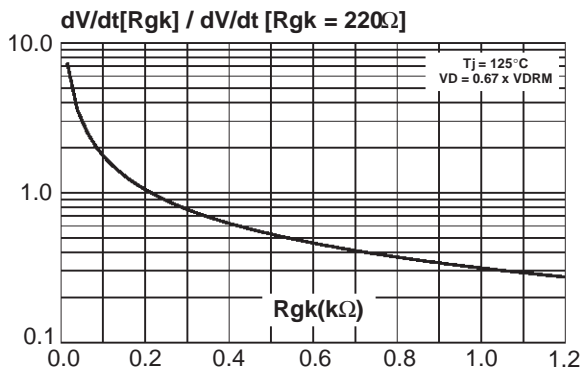
**Fig. 3-2:** Relative variation of thermal impedance junction to ambient versus pulse duration (recommended pad layout, FR4 PC board).



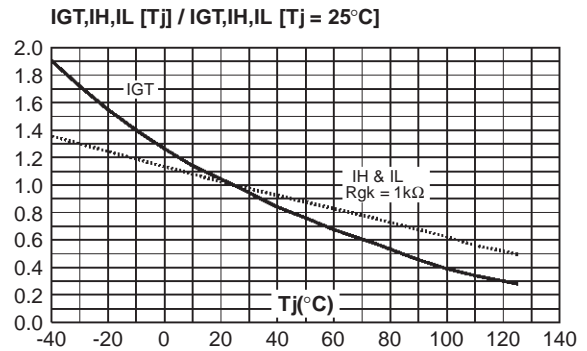
**Fig. 4-2:** Relative variation of gate trigger current, holding current and latching current versus junction temperature for TN12 & TYN series.



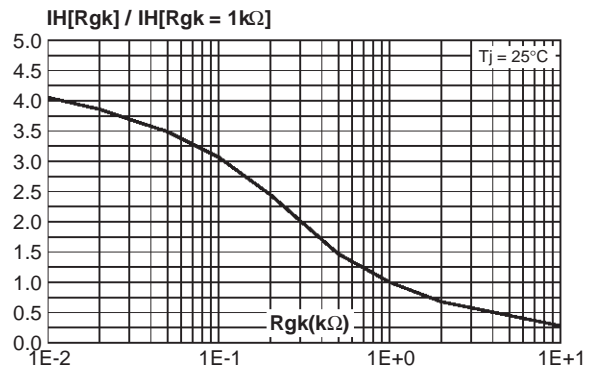
**Fig. 6:** Relative variation of dV/dt immunity versus gate-cathode resistance (typical values) for TS12 series.



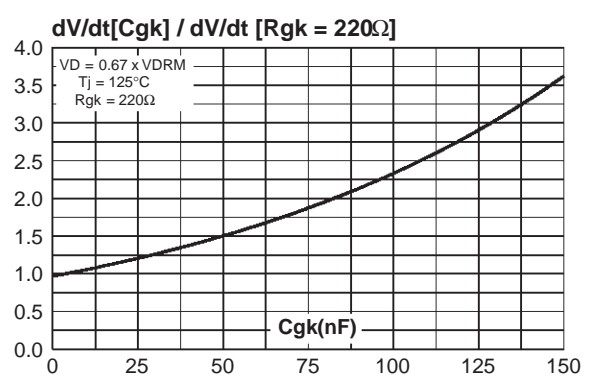
**Fig. 4-1:** Relative variation of gate trigger current, holding current and latching versus junction temperature for TS12 series.



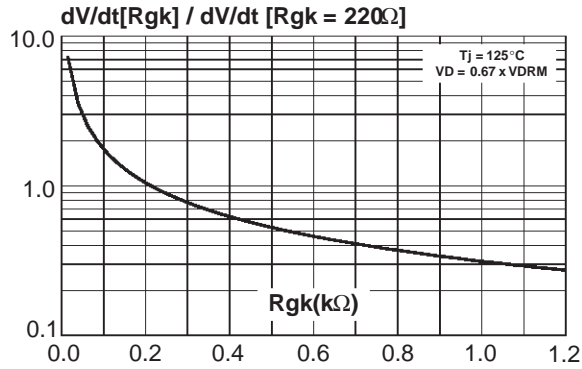
**Fig. 5:** Relative variation of holding current versus gate-cathode resistance (typical values) for TS12 series.



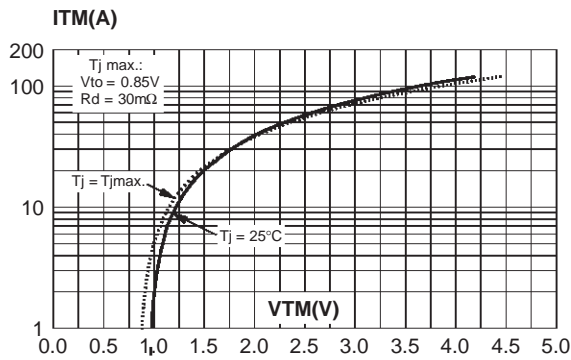
**Fig. 7:** Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values) for TS12 series.



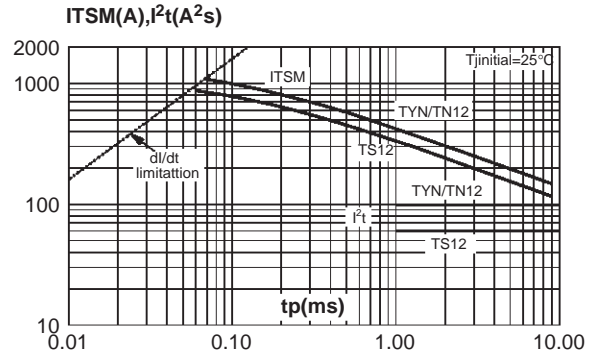
**Fig. 8:** Surge peak on-state current versus number of cycles (TS12/TN12/TYN).



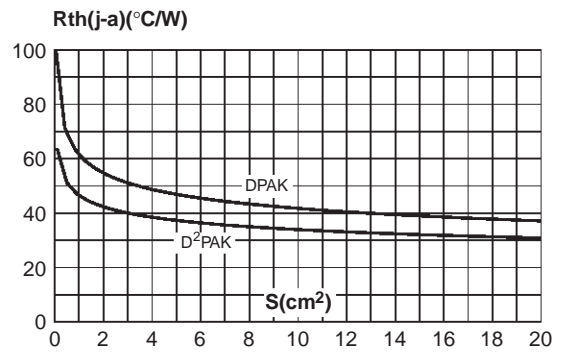
**Fig. 10:** On-state characteristics (maximum values).



**Fig. 9:** Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10$  ms, and corresponding values of  $I_t$ .

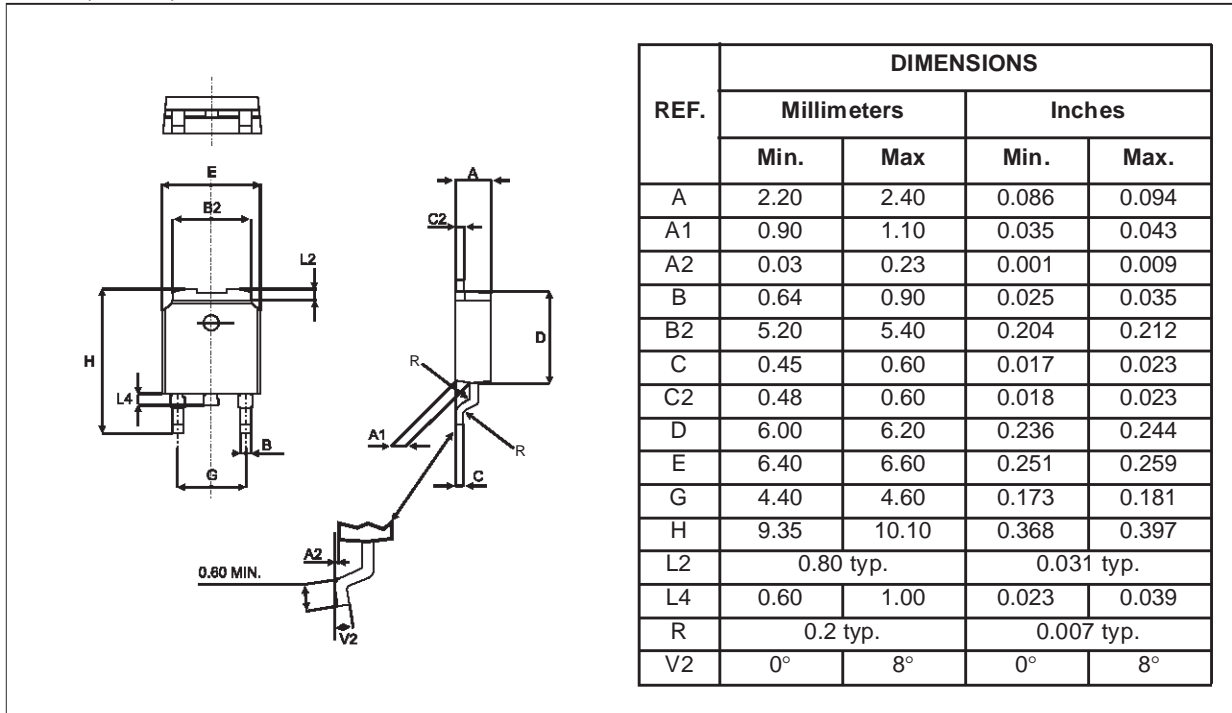


**Fig. 11:** Thermal resistance junction to ambient versus copper surface under tab (Epoxy printed circuit board FR4, copper thickness: 35  $\mu\text{m}$ ).



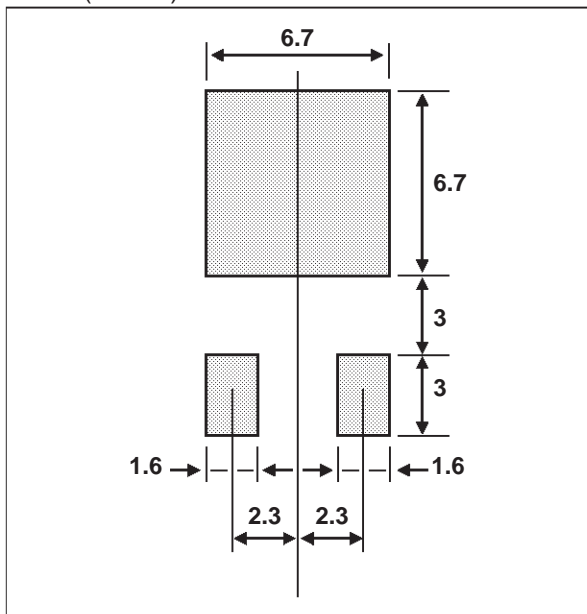
**PACKAGE MECHANICAL DATA**

DPAK (Plastic)



**FOOTPRINT DIMENSIONS (in millimeters)**

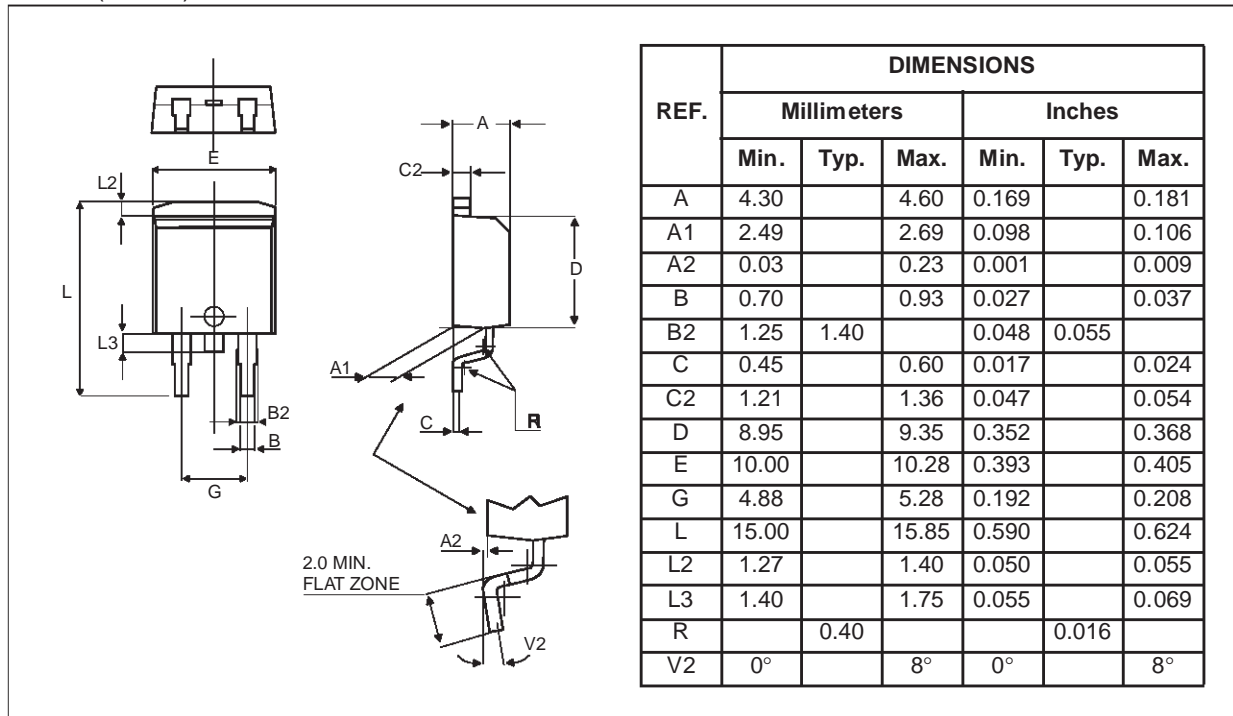
DPAK (Plastic)



## TN12, TS12 and TYNx12 Series

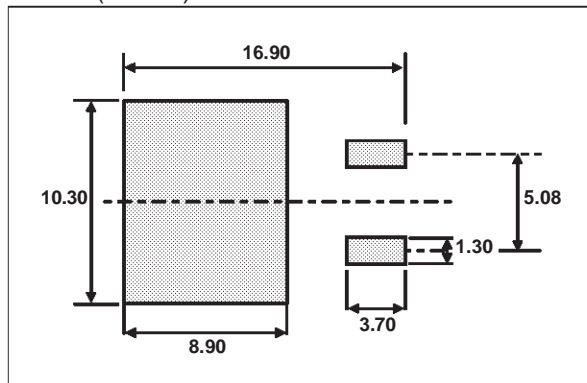
### PACKAGE MECHANICAL DATA

D<sup>2</sup>PAK (Plastic)



### FOOTPRINT DIMENSIONS (in millimeters)

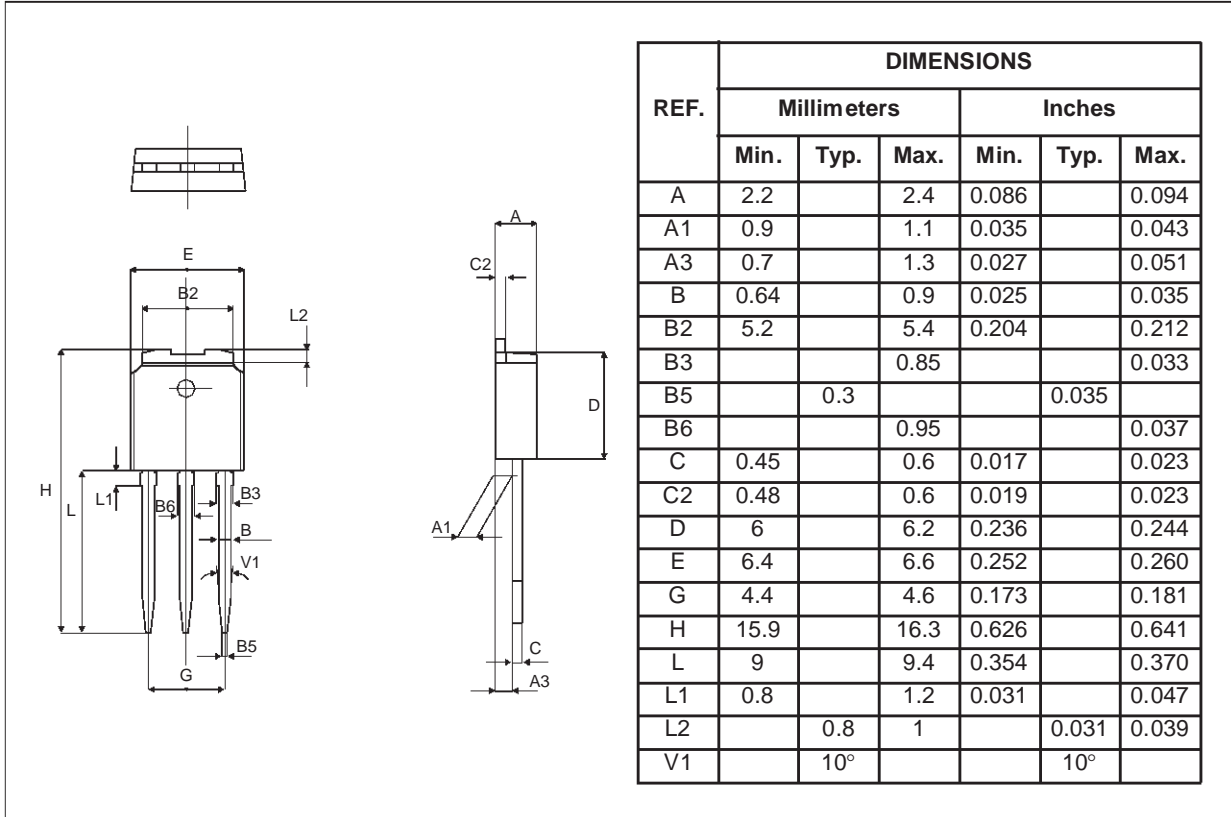
D<sup>2</sup>PAK (Plastic)





PACKAGE MECHANICAL DATA

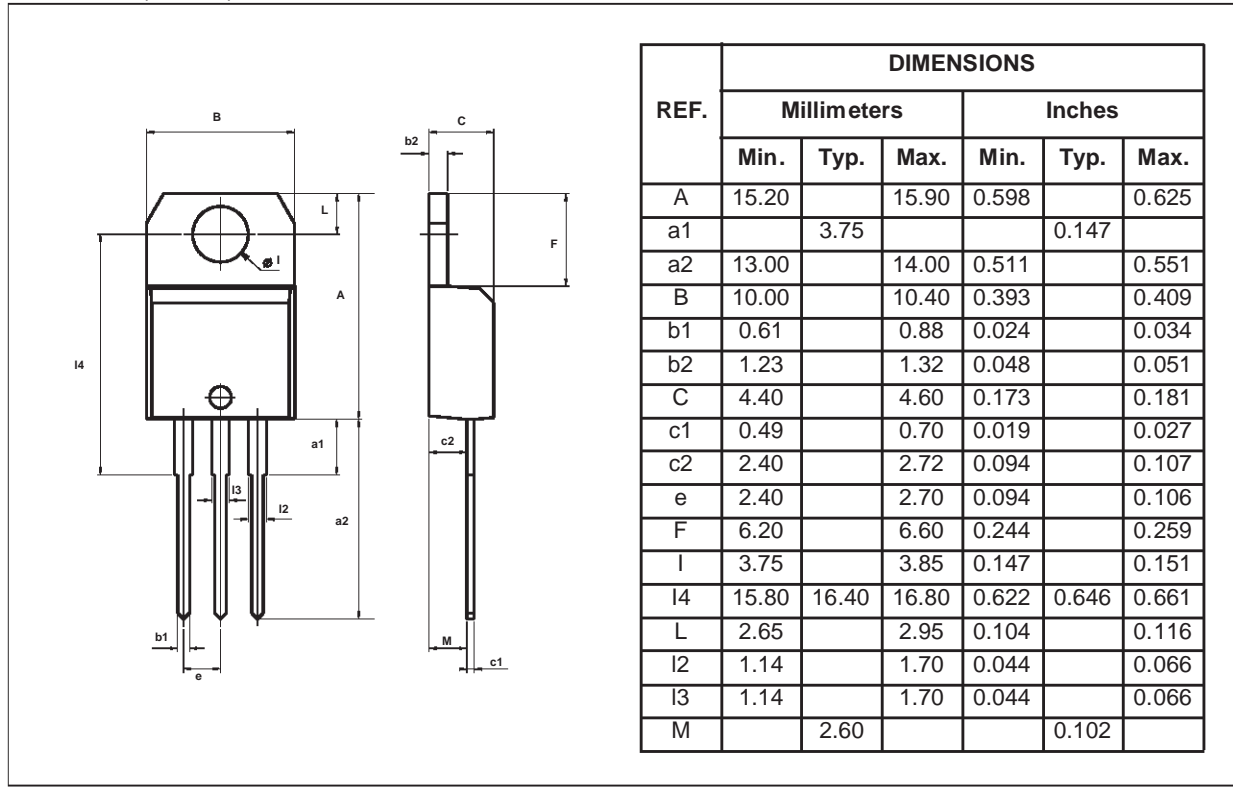
IPAK (Plastic)



## TN12, TS12 and TYNx12 Series

### PACKAGE MECHANICAL DATA

TO-220AB (Plastic)



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